4.1.5 TS3000 Standalone Thermal Sensor Component

Mobile Platform Memory Module Thermal Sensor Component Specification. Revision 1.03

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1 Device Standard

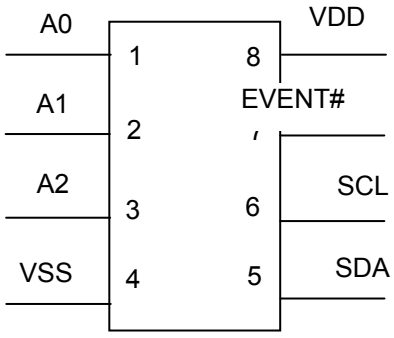
The TS3000av is a Temperature Sensor device designed to operate in one of three voltage ranges, 1.7-3.6 V, 2.3-3.6 V, or 3.0-3.6 V. All devices meet the thermal performance characteristics, and the 2.3-3.6 V or 3.0-3.3 V nominal devices shall operate the I^2C bus at a 400 kHz maximum. Devices are intended to interface to I^2C buses which have multiple devices on a shared bus, and must be uniquely addressed on this bus. A substantial reduction in supply current may be achieved using the software programmed shutdown mode. The device family contains two temperature grades designated with a second letter appended to the part number.

Common Features summary:

TS3000av Variations						
Base Part Number		a	Sensor Accuracy		v	Single Supply Voltage
TS3000		B	0.5 ºC typ from 75-95 ºC		1	1.7 to 3.6 V
			1.0 ºC typ from 40-125 ºC		2	2.3 to 3.6 V
			2.0 ºC typ from -20-125 ºC		3	3.0 to 3.6 V
		C	1.0 ºC typ from 75-95 ºC			
			2.0 ºC typ from 40-125 ºC			
			3.0 ºC typ from -20-125 ºC			

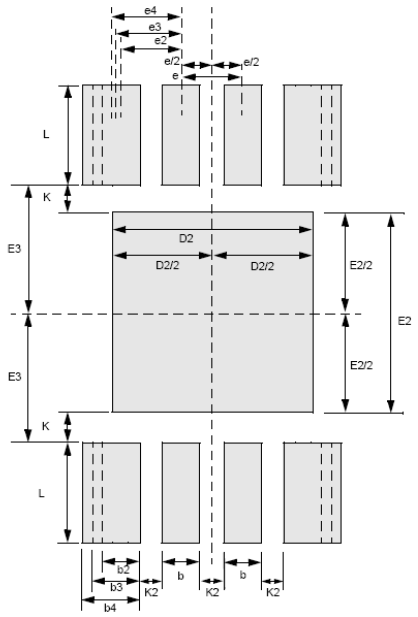
2 Memory Module Thermal Sensor

The Sensor component shares the SMBus/I^2C with the Serial Presence Detect EEPROM (SPD) on the memory module. The recommended pin out (package) and footprint (PCB Layout) is as follows:



Remote TS
Matches SPD
Top View
LLP/MLP/PSON 8-pin (MO-229 V/WEED-7, V/WCED-3); TSSOP-8

Figure 1 - Pinout (and Package) Options for Thermal Sensor Components



The table lists three variations of landing pattern implementations, ranked as "Preferred", "Intermediate", and "Minimum Acceptable".

TABLE 18. Parameters for SPD Common Landing Pattern

Parameter	Description	Dimension			Notes
		Min	Nom	Max	
D2	Heat paddle width	1.40	-	1.60	
E2	Heat paddle height	1.40	-	1.60	
E3	Heat paddle centerline to contact inner locus	1.00	-	1.05	
L	Contact length	0.70	-	0.80	
K	Heat paddle to contact keepout	0.20	-	-	
K2	Contact to contact keepout	0.20	-	-	
e	Contact centerline to contact centerline pitch for inner contacts	-	0.50	-	
b	Contact width for inner contacts	0.25	-	0.30	
e2	Landing pattern centerline to outer contact centerline, "minimum acceptable" option	-	0.50	-	1
b2	Corner contact width, "minimum acceptable" option	0.25	-	0.30	1
e3	Inner contact centerline to outer contact centerline, "intermediate" option	-	0.55	-	2
b3	Corner contact width, "intermediate" option	0.35	-	0.40	2
e4	Landing pattern centerline to outer contact centerline, "preferred" option	-	0.60	-	3
b4	Corner contact width, "preferred" option	0.45	-	0.50	3

Notes:
1. Minimum acceptable option to be used when routing prevents preferred or intermediate width contact.
2. Intermediate option to be used when routing prevents preferred width contact.
3. Preferred option to be used when possible.

Figure 2 - Recommended Landing Pattern Options (PCB Footprint)
See JESD21C-4.1.2 for details. All dimensions in mm

Table 1 – Pinout of Thermal Sensor

Pin	Description
Power Supply	
VDD	Positive Supply, Power
VSS	Negative Supply, Ground
SMBus/I^{2}C Serial Interface	
SDA	SMBus/I^{2}C Data pin
SCL	SMBus/I^{2}C Clock pin
A0/A1/A2	Lower bits of the SMBus/I^{2}C Slave Address
Thermal Sensor	
EVENT#	Active Low. Open Drain EVENT# output pin. Driven low on comparator level, or Alert Interrupt

3 Key Features

- Temperature accuracy
  - TS3000Cv = Typical accuracy of ±1.0 °C for the active range from 70 ~ 95 °C.
  - TS300Cv = Typical accuracy of ±2.0 °C for other monitor ranges from 40 ~ 125 °C.
  - TS3000Bv = Support for higher accuracy of ±0.5 °C (typical) over the active range.
- Ambient temperature (T_A) sense through an operating range of -20 to +125 °C.
- Temperature sample rate minimum of 8 samples/s.
- Operating voltage range
  - TS3000a1 = 1.7 V to 3.6 V.
  - TS3000a2 = 2.3 V to 3.6 V.
  - TS3000a3 = 3.0 V to 3.6 V.
- Low operating current (~500 uA typical).
- Selectable 0, 1.5 °C, 3 °C, 6 °C Hysteresis.
- Package
  - LLP/MLP/PSON or TSSOP 8 pin (E = 3 mm D = 3 mm or E = 3 mm D = 2 mm) package for all memory modules including SO-DIMMs .
  - JEDEC Registration MO-229 V/WEED-7 (3 mm by 3 mm) or V/WCED-3 (2 mm by 3 mm) footprint.
  - Exposed DAP to be connected to V_{SS} to enhance thermal conductivity.
- Security bits for robust operation.
- SMBus/I^{2}C compatible serial interface supporting up to 400 kHz bus speeds.
- Dual purpose event pin: Comparator or Interrupt (compatible with SMBus Alert) mode.
- Since this device could be used in memory modules at other operating voltages, the thermal sensor is not required to operate at any other voltage range than specified here. However, it is required that

the thermal sensor does not inhibit any operation of the module (i.e., bus activity) while the module operates at other voltages.

- Since this device will reside on the same address bus as other devices, it is required to allow up to 10 V on the A0 pin.

4 Electrical Characteristics

Operating Conditions for TS3000av Family

Symbol	Parameter	TS3000a1		TS3000a2		TS3000a3		Units
		Min	Max	Min	Max	Min	Max	
VDD	Supply Voltage	1.7	3.6	2.3	3.6	3.0	3.6	V

Table 2. Specifications at T_A = −20 °C to +125 °C , unless otherwise noted

Parameter	Min	Typ	Max	Unit	Test Conditions
POWER SUPPLY					$V_{DDMIN} \le V_{DD} \le V_{DDMAX}$
Allowable voltage on pin A0 (pin 1)			10	V	Pin A0 must be capable of supporting up to 10 V consistent with EE1002 and TSE2002av device family specifications
Leakage on pin A0 in overvoltage state		500		uA	
Average Operating Supply Current, I_{DD}			500	µA	
TEMPERATURE-TO-DIGITAL CONVERTER					
Local Sensor Accuracy (C grade)[1]		±1.0	±2.0	°C	75 °C ≤ T_A ≤ 95 °C, Active Range
		±2.0	±3.0	°C	40 °C ≤ T_A ≤ 125 °C, Monitor Range
		±3.0	±4.0	°C	−20 °C ≤ T_A ≤ 125 °C
Local Sensor Accuracy (B grade)[1]		±0.5	±1.0	°C	75 °C ≤ T_A ≤ 95 °C, Active Range
		±1.0	±2.0	°C	40 °C ≤ T_A ≤ 125 °C, Monitor Range
		±2.0	±3.0	°C	−20 °C ≤ T_A ≤ 125 °C
Resolution		0.25		°C	
Conversion Time			125	ms	Worst case conversion time

[1] Refer to individual vendor datasheets for explanation of accuracy testing methodology.

Table 2. Specifications at T_A = −20 °C to +125 °C , unless otherwise noted					
SMBus/I^{2}C INTERFACE					
Logic Input High Voltage, V_{IL} (SCL, SDA)	-0.5		0.3 * V_{DD}	V	
Logic Input Low Voltage, V_{IH} (SCL,SDA)	0.7 * V_{DD}		V_{DD} + 1	V	
Logic Output Low Voltage, V_{OL} (SCL, SDA)			0.4	V	I_{PULL_UP} of 350 uA
SMBus/I^{2}C Output Low Sink Current	6			mA	SDA Forced to 0.6 V
Logic Input Current, I_{IH}, I_{IL}	−5		+5	µA	
Input Hysteresis[2]	0.10 * V_{DD}			V	V_{DD} < 2.2 V
	0.05 * V_{DD}			V	$V_{DD} \geq$ 2.2V
SMBus/I^{2}C Input Capacitance (SCL, SDA)		5		pF	
SMBus/I^{2}C Clock Frequency	10		100	kHz	V_{DD} < 2.2 V
	10		400	kHZ	$V_{DD} \geq$ 2.2V
Pulse width of spikes which must be suppressed by the input filter	n/a		n/a	ns	f ≤ 100 KHz
	0		50	ns	f > 100 KHz

4.1 SMBus/I^{2}C

4.1.1 SMBus/I^{2}C Communications

The data registers in this device are selected by the Pointer Register. At power-up the Pointer Register is set to “00”, the location for the Capability Register. The Pointer Register latches the last location it was set to. Each data register falls into one of three types of user accessibility:

1. Read only

2. Write only

3. Write/Read same address

A Write to this device will always include the address byte and the pointer byte. A write to any register, other than the pointer register, requires two data bytes.

Reading this device can take place either of two ways:

1. If the location latched in the Pointer Register is correct (most of the time it is expected that the Pointer Register will point to one of the Read Temperature Registers because that will be the data most frequently read), then the read can simply consist of an address byte, followed by retrieving the two data bytes.

[2] Optional.

2. If the Pointer Register needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (Ack) or No Acknowledge (No Ack) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). It takes this device 125 ms to measure the temperature.

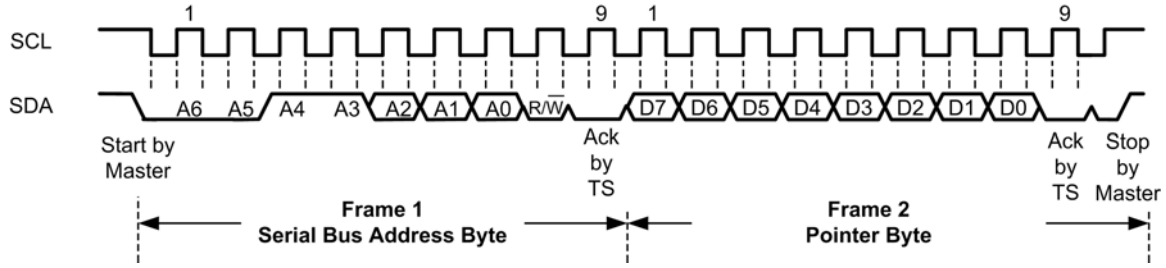


Figure 3 - SMBus/I^{2}C write to the pointer register

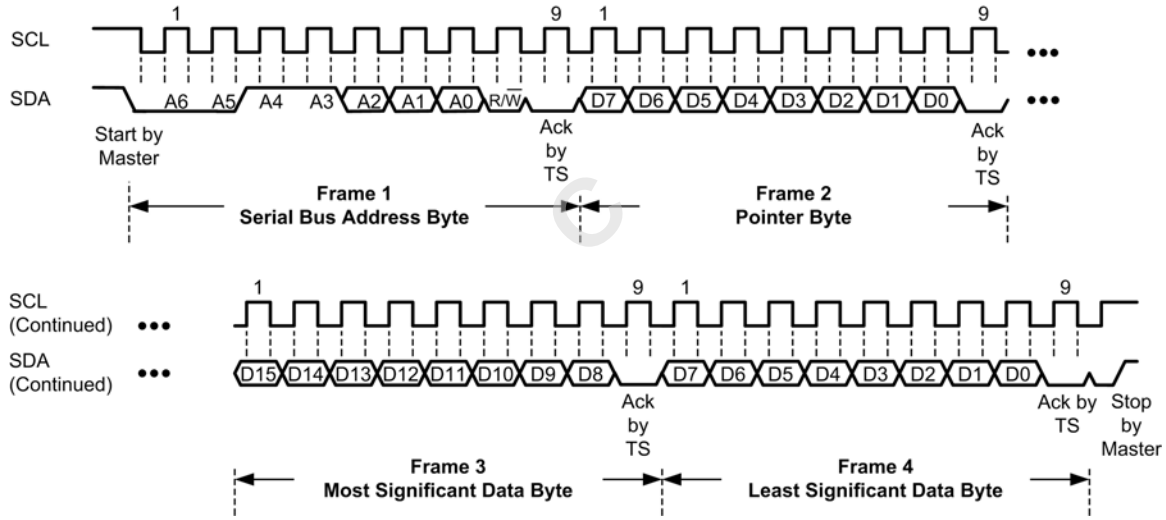


Figure 4 - SMBus/I^{2}C write to the pointer register followed by a write data word

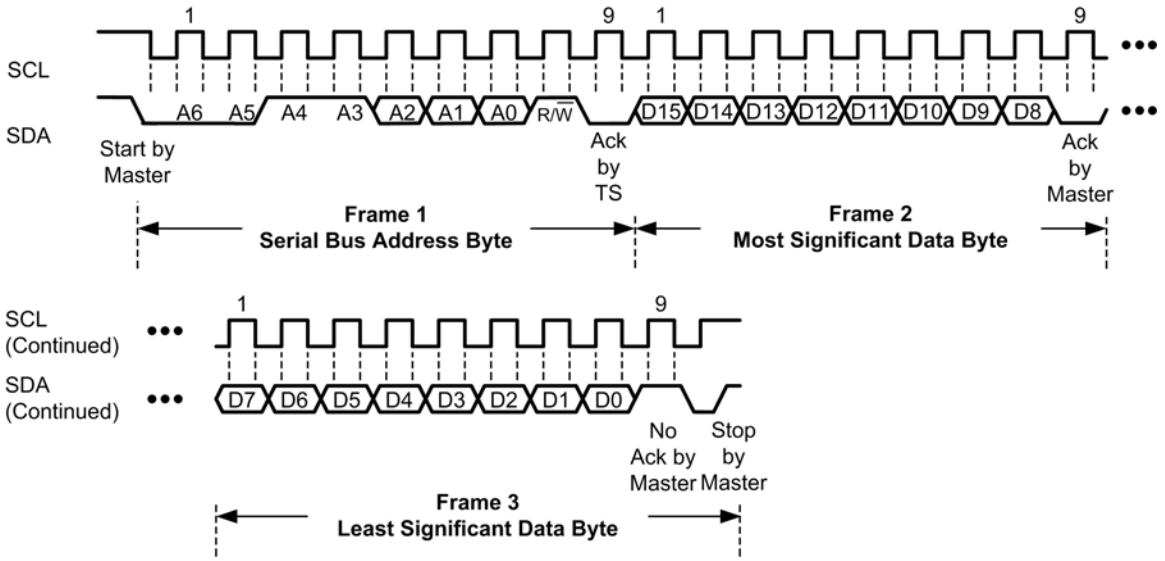


Figure 5 - SMBus/I^{2}C word read from register with a preset pointer

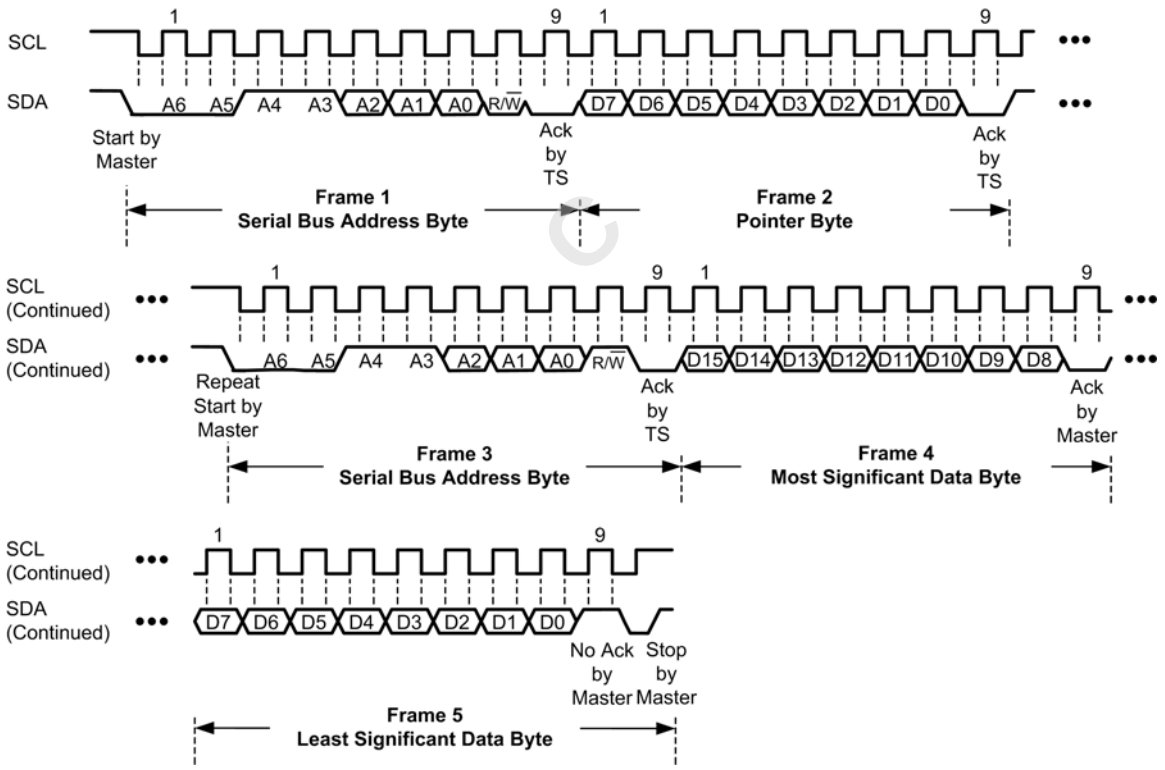


Figure 6 - SMBus/I^{2}C write to pointer register followed by a repeat start and an immediate data word read

4.1.2 SMBus/I^{2}C Slave Sub-Address Decoding

The physical address for TS is different than that used by current SPD devices. The physical address for thermal sensor is “0 0 1 1 A2 A1 A0 RW” in binary, where A2, A1, A0 are the three slave sub-address pins, and the least significant bit “RW” is the Read/Write flag.

Assuming the slave base address of the SPD+TS interface is fixed, for example at 0x30, then the pins set the sub-address bits of the slave address, allowing the device to be located anywhere within 8 slave address locations, for example from 0x30 to 0x3E.

Slave Address	A2	A1	A0
x0	0	0	0
x2	0	0	1
x4	0	1	0
x6	0	1	1
x8	1	0	0
xA	1	0	1
xC	1	1	0
xE	1	1	1

Table 3 – Slave Address Decoding

The meaning of the A0/A1/A2 pin states is as follows:

0	Pull-down to Thermal Sensor V_{SS}
1	Pull-up to Thermal Sensor V_{DD}

4.1.3 SMBus/I²C AC Timing Consideration

In order for this device to be both SMBus and I^2C compliant, the device complies with a subset of each specification. This requires a few minor considerations to ensure interoperability. The time out requirements of SMBus are optional for this device. The minimum clock frequency of SMBus is a required feature. Note that the minimum data hold time ($T_{HD:DAT}$) of 200 ns is smaller than the 300 ns of the SMBus specification. With these minor considerations, this device is capable of co-existing with devices on either an SMBus or an I^2C bus.

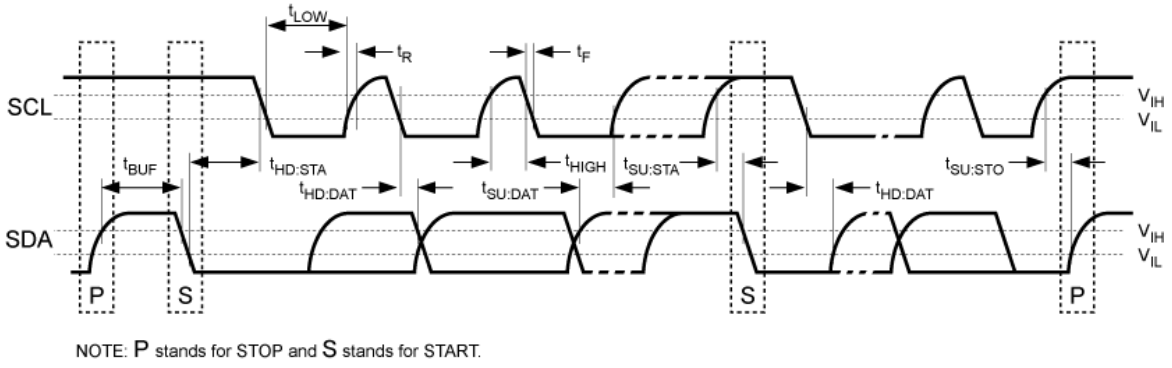


Figure 7 – SMBus / I^2C timing diagram

Table 4 – AC Timing Parameters for SMBus and I^2C Compatibility

		VDD < 2.2 V		VDD ≥ 2.2 V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{SCL}	Clock frequency	10	100	10	400	KHz
t_{BUF}	Bus free time between Stop (P) and Start (S) condition	4700		1300		ns
$t_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	4000		600		ns
$t_{SU:STA}$	Repeated Start Condition setup time	4700		600		ns
t_{HIGH}	Clock high period	4000		600		ns
t_{LOW} [3]	Clock low period	4700		1300		ns
t_f	Clock/Data Fall Time		300	20	300	ns
t_r	Clock/Data Rise Time		1000	20	300	ns
$t_{TIMEOUT}$ [4]	Detect Clock Low Timeout, Capabilities Register bit 6 = 0	10	60	10	60	ms
$t_{TIMEOUT}$	Detect Clock Low Timeout, Capabilities Register bit 6 = 1	25	35	25	35	ms
$t_{SU:DAT}$	Data setup time	250		100		ns
$t_{HD:DI}$	Data input hold time	0		0		ns
$t_{HD:DAT}$	Data output hold time	200	3450	200	900	ns
$t_{SU:STO}$	Stop Condition setup time	4000		600		ns

[3] TS3000 family devices shall not initiate clock stretching, which is an optional I^2C bus feature.

[4] Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT,MIN}$. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. Typical device examples include the host controller, and embedded controller and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds SCL low for $t_{TIMEOUT,MAX}$ or longer. Note that the timeout value supported is described in the Capabilities Register.

For complete details of these parameters, consult the following specifications:

- *System Management Bus* (SMBus) version 2.0, SBS Implementer's Forum, 3 August 2000[5]
- *The I²C-bus and how to use it*, Philips Semiconductors document #98-8080-575-01.

5 Description

The thermal sensor continuously monitors the temperature and updates the temperature data at least eight times per second. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

SMBus/I^2C slave address selection pins allow up to 8 such devices to co-exist on the same bus. This means that up to 8 memory modules can be supported given each module has one such slave device address slot.

After initial power-on, the configuration registers are set to the default values. Software can write to the configuration register to set bits as per the bit-definitions in the following section.

5.1 EVENT# Pin Functionality

EVENT# is an open drain output and requires a pull-up resistor to VDD on the system motherboard or incorporated into the master controller.

The diagram below shows the 3 differently-defined outputs of EVENT# correspondent to the temperature change. EVENT# can be programmed to be one of the three output modes.

If in Interrupt Mode and the temperature reaches the critical temperature, the device switches to the comparator mode automatically and asserts the EVENT# output. When the temperature drops below the critical temperature, the part switches back to either Interrupt, or Comparator mode, as programmed in the "Configuration" Register. Note that Figure 8 is drawn with no hysteresis, but the values programmed into register 0x01 bits 10:9 affect the operation of the event trigger points. See Figure 9 for further explanation of hysteresis functionality.

[5] TS3000 devices are not required to support the SMBus ALERT function.

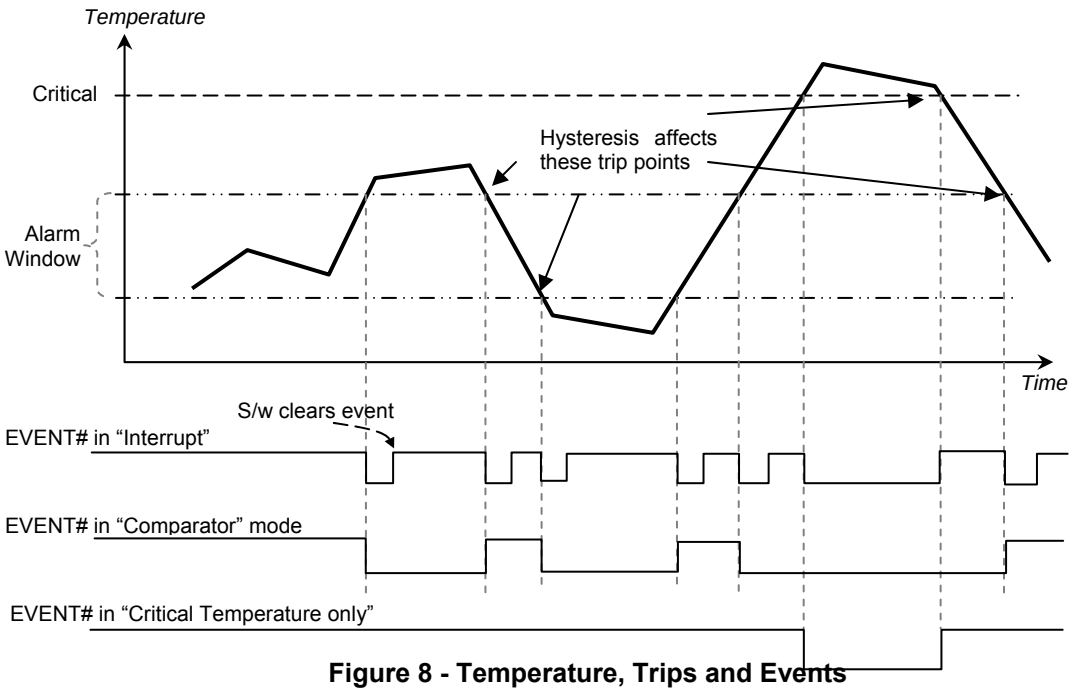


Figure 8 - Temperature, Trips and Events

5.1.1 Event Thresholds

All event thresholds use hysteresis as programmed in register 0x01 bits 10:9 to set when they deassert (stop driving).

5.1.1.1 Alarm Window Trip

The device provides a comparison window with an upper temperature trip point in the Alarm Upper Boundary Register, and a lower trip point in the Alarm Lower Boundary Register. When enabled, the EVENT# output will be triggered whenever entering, or exiting (crossing above or below) the Alarm Window.

5.1.1.2 Critical Trip

The device can be programmed in such a way that the EVENT# output is only triggered when the temperature exceeds critical trip point. The Critical temperature setting is programmed in Critical Temperature Register. When the temperature sensor reaches the critical temperature value in this register, the device is automatically placed in comparator mode meaning that the Critical Event output cannot be cleared through software setting the “Clear Event” bit.

5.1.2 Interrupt Mode

After an Event occurs, Software may write a one (‘1’) to the “Clear Event” bit in the Configuration Register to de-assert the EVENT# Interrupt output, until the next trigger condition occurs.

5.1.3 Comparator Mode

Reads/writes on the device registers will not affect the EVENT# output in comparator mode. The EVENT# signal will remain asserted until the temperature drops outside the range, or the range is re-programmed such that the current temperature is outside the range.

6 Registers

Address (Hex)	Name	Power-On Default
Not Applicable	Address Pointer	Undefined
00	Capability Register	(0x0001)
01	Configuration Register	(0x0000)
02	Alarm Temperature Upper Boundary Trip Register	(0x0000)
03	Alarm Temperature Lower Boundary Trip Register	(0x0000)
04	Critical Temperature Trip Register	(0x0000)
05	Temperature Register	Undefined
06	Manufacturer's ID register	(0x0000)
07	Device ID / Revision Register	(0x0000)
08-0F	Vendor-defined Registers	(0x0000)

6.1 Pointer Register (Write only)

This 8-bit register selects which of the 16-bit registers is accessed in subsequent read/writes. Address space between 0x08 and 0xFF may be used for vendor specific registers or test registers.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	Register Select	Register Select	Register Select	Register Select

Bit2	Bit1	Bit0	Register
0	0	0	Capability Register
0	0	1	Configuration register
0	1	0	Alarm temperature upper boundary trip register
0	1	1	Alarm temperature lower boundary trip register
1	0	0	Critical temperature trip register
1	0	1	Temperature Register
1	1	0	Manufacturer ID
1	1	1	Device ID/Revision

6.2 Capability Register (Read Only)

This indicates the capabilities of the Thermal Sensor.

Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
EVSD	TMOUT	VHV	TRES1	TRES0	Wider Range	Higher Precision	Has Alarm & Critical Trips

Bit	**Definition**
0	**Basic Capability** 1 - Has Alarm & Critical Trips capability (required)
1	**Accuracy** 0 – Default, accuracy ±2 °C over the active and ±3 °C monitor ranges 1 - High accuracy ±1 °C over the active and ±2 °C monitor ranges
2	**Wider Range** 0 - Values lower than 0 °C will be clamped and represented as binary value 0 1 - Can read temperatures below 0 °C and set sign bit accordingly
4:3	**Temperature Resolution** 00 – 0.5 °C LSB 01 – 0.25 °C LSB 10 – 0.125 °C LSB 11 – 0.0625 °C LSB
5	**High Voltage Standoff for pin A0** 0 – Default 1 – This part can support a voltage up to 10 V on the A0 pin consistent with EE1002 and TSE2002av device family specifications
6	**Bus Timeout Period** 0 – Default. Parameter tTIMEOUT is supported within the range of 10 to 60 ms. 1 – Parameter tTIMEOUT is supported within the range of 25 to 35 ms (SMBus compatible).
7	**EVENT With Shutdown Action** 0 – Default. The EVENT# output freezes in its current state when entering shutdown. Upon exiting shutdown, the EVENT# output remains in the previous state until the next thermal sample is taken, or possibly sooner if EVENT# is programmed for comparator mode. 1 – The EVENT# output is deasserted (not driven) when entering shutdown, and remains deasserted upon exit from shutdown until the next thermal sample is taken, or possibly sooner if EVENT# is programmed for comparator mode.
15:8	0 - Reserved for future use. Must be zero.

6.3 Configuration Register (read/write)

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
RFU	RFU	RFU	RFU	RFU	Hysterisis		Shutdown mode
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Critical Lock Bit	Alarm Lock Bit	Clear Event	Event Output Status	Event Output Control	Critical Event Only	EVENT# Polarity	Event Mode

Bit	Description
0	**Event Mode** 0 - Comparator output mode (default) 1 - Interrupt mode When either of the lock bits is set, this bit cannot be altered until unlocked.
1	**EVENT# Polarity** 0 - Active Low (default) 1 - Active High When either of the lock bits is set, this bit cannot be altered until unlocked
2	**Critical Event Only** 0 - Event output on Alarm or Critical temperature event (default) 1 - Event only if temperature is above the value in the critical temperature register When the Alarm Window lock bit is set, this bit cannot be altered until unlocked
3	**Event Output Control** 0 - Event Output Disabled (default) 1 - Event Output Enabled When either of the lock bits is set, this bit cannot be altered until unlocked.
4	**Event Status (read only)** 0 - Event Output condition is not being asserted by this device 1 - Event Output pin is being asserted by this device due to Alarm Window or Critical trip condition The actual event causing the event can be determined from the Read Temperature register. Interrupt Events can be cleared by writing to “Clear Event” bit. Writing to this bit will have no effect.
5	**Clear Event (write only)** 0 - No effect 1 - Clears active event in Interrupt Mode. Writing to this register has no effect in Comparator Mode. When read, this bit will always return zero ‘0’
6	**Alarm Window Lock bit** 0 - Alarm Trips are not locked and can be altered (default) 1 - Alarm Trip register settings cannot be altered This bit is initially cleared. When set this bit will return a 1, and remain locked until cleared by internal power-on reset. These bits can be written with a single write and do not require double writes.
7	**Critical Trip Lock bit** 0 - Critical Trip is not locked and can be altered (default) 1 - Critical Trip register settings cannot be altered This bit is initially cleared. When set this bit will return a 1, and remain locked until cleared by internal power-on reset. These bits can be written with a single write and do not require double writes.

8	**Shutdown Mode** 0 - Enabled TS (default) 1 - Shutdown TS When shutdown, the thermal sensing device and A/D converter are disabled to save power, no events will be generated. When either of the lock bits is set, this bit cannot be set until unlocked. However it can be cleared at any time. The EVENT# pin is de-asserted. The device continues to process commands normally.
10:9	**Hysteresis Enable** 00 - Disable Hysteresis 01 - Enable Hysteresis at 1.5 °C 10 - Enable Hysteresis at 3 °C 11 - Enable Hysteresis at 6 °C When enabled, hysteresis is applied to temperature movement around trigger points. For example, consider the behavior of the "Above Alarm Window" bit (Bit 14 of the Temperature Register) when the hysteresis is set to 3 °C. As the temperature rises, Bit 14 will be set to 1 (temperature is above the alarm window) when the Temperature Register contains a value that is greater than the value in the Alarm Temperature Upper Boundary Register. If the temperature decreases, Bit 14 will remain set until the measured temperature is less than or equal to the value in the Alarm Temperature Upper Boundary Register minus 3 °C. See Figure 8 for more detail. Similarly, the "Below Alarm Window" bit (Bit 13 of the Temperature Register) will be set to 0 (temperature is equal to or above the Alarm window lower boundary trip temperature) when the value in the temperature register is equal to or greater than the value in the Alarm Temperature Lower Boundary Register. As the temperature decreases, Bit 13 will be set to 1 when the value in the Temperature Register is less than the value in the Alarm Temperature Lower Boundary Register minus 3 °C. Note that hysteresis is also applied to EVENT# pin functionality. When either of the lock bits is set, these bits cannot be altered.

T_U = Value stored in Alarm Temperature Upper Boundary Trip Register
T_L = Value stored in Alarm Temperature Lower Boundary Trip Register
Hyst = Absolute value of selected hysteresis

	Below Alarm Window Bit		Above Alarm Window Bit	
	Temperature slope	Threshold Temperature	Temperature Slope	Temperature
Sets	Falling	T_L -Hyst	Rising	T_H
Clears	Rising	T_L	Falling	T_H -Hyst

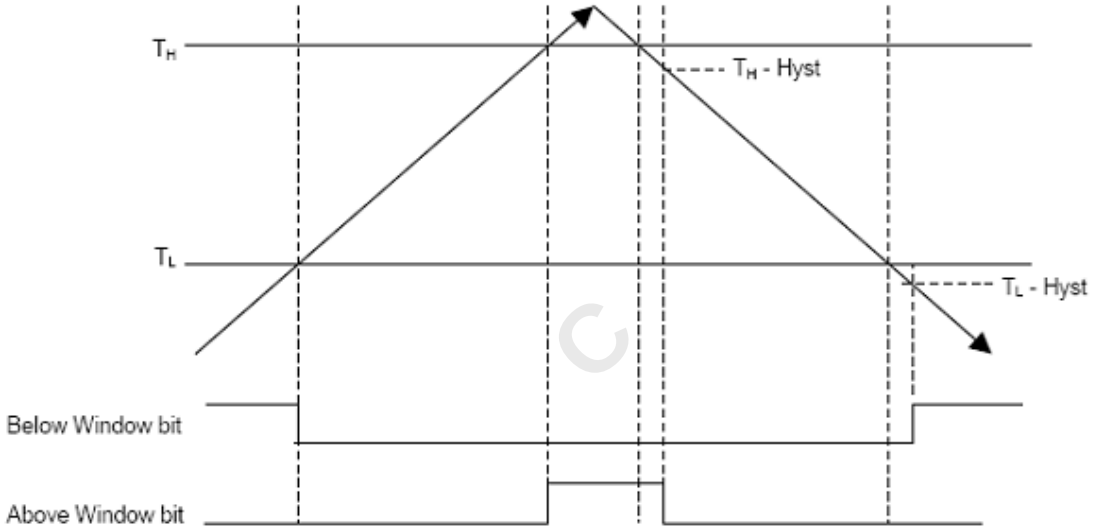


Figure 9 – Hysteresis

6.4 Temperature Format

The 16-bit value used in the following Trip Point Set & Temperature Read-Back registers is 2's complement with the Least Significant Bit equal to 0.0625 °C. For example:

- A value of 0x019C will represent 25.75 °C
- A value of 0x07C0 will represent 124 °C
- A value of 0x1E74 will represent –25.75 °C

The resolution of 0.0625 °C is optional. It is mandatory to support a resolution of at least 0.25 °C. All unused bits of the resolution will be set to zero. The most significant bit will have a resolution of 128 °C.

The Upper 3 bits indicate Trip Status based on the current temperature, and are not affected by the status of the EVENT# Output.

6.5 Temperature Trip Point Registers

6.5.1 Alarm Temperature Upper Boundary Register (read/write)

The value is the upper threshold temperature value for Alarm Mode. The data format is 2's complement with one LSB = 0.25 °C. RFU bits are not supported and will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	Sign MSB										LSB	RFU	RFU
			Alarm Window Upper Boundary Temperature												

6.5.2 Alarm Temperature Lower Boundary Register (read/write)

The value is the lower threshold temperature value for Alarm Mode. The data format is 2's complement with one LSB = 0.25 °C. RFU bits are not supported and will always report zero. Interrupts will respond to the presently programmed boundary values. If boundary values are being altered in-system, it is advised to turn off interrupts until a known state can be obtained to avoid superfluous interrupt activity.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	Sign MSB										LSB	RFU	RFU
			Alarm Window Lower Boundary Temperature												

6.5.3 Critical Temperature Register (read/write)

The value is the critical temperature. The data format is 2's complement with one LSB = 0.25 °C. RFU bits are not supported and will always report zero.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	Sign MSB										LSB	RFU	RFU
			Critical Temperature Trip Point												

6.6 Temperature Register (read only)

The value is the current sensed temperature.

The data format is 2's complement with one LSB = 0.0625 °C. The resolution of 0.0625 °C is optional. It is mandatory to support a resolution of at least 0.25 °C. All unused bits of the resolution will be set to zero. The most significant bit will have a resolution of 128 °C.

The Trip Status bits represent the internal temperature trip detection, and are not affected by the status of the Event or Configuration bits e.g. Event Output Control, Clear Event. If neither Above or Below are set (i.e. both are 0) then the current Temperature is exactly within the alarm window boundaries as defined in section 5.3.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Above Critical Trip	Above Alarm Window	Below Alarm Window	Sign MSB												LSB
			Temperature												

Bit	Definition
13	**Below Alarm Window** 0 - Temperature is equal to or above the Alarm window lower boundary temperature 1 - Temperature is below the Alarm window
14	**Above Alarm Window** 0 - Temperature is equal to or below the Alarm window upper boundary temperature 1 - Temperature is above the Alarm window
15	**Above Critical Trip** 0 - Temperature is below the critical temperature setting 1 - Temperature is equal to or above the critical temperature setting

6.7 Manufacturer ID Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
0	0	0	0	0	0	0	0
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0	0	0	0	0	0	0	0

This manufacturer ID matches that assigned to a vendor within the PCI SIG. This register may be used to identify the manufacturer of the device in order to perform manufacturer specific operations. Manufacturer IDs can be found at www.pcisig.com.

6.8 Device ID and Revision Register

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
DEVICE ID							
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
DEVICE REVISION							

The Device ID and Device Revision are assigned by the manufacturer of the device. The Device Revision will start at 0 and be incremented by one whenever an update to the device is issued by the manufacturer of the device.

6.9 Packaging Options

Three package options will be supported: the TSSOP 8-lead, the 3x3 mm MO-229 V/WEED-7, and the 2x3 mm MO-229 V/WCED-3. The common landing pattern shown in Figure 2 supports either MO-229 option and is used in all JEDEC standard reference module designs. It will be up to the discretion of the IC vendors as to which of these packages they support.