## 4.1.4  Definition of the TSE2002av Serial Presence Detect (SPD) EEPROM with Temperature Sensor (TS) for Memory Module Applications

### 1. SCOPE

This standard defines the specifications of interface parameters, signaling protocols, and features for Serial Presence Detect (SPD) EEPROMs and Temperature Sensor (TS) as used for memory module applications. The designation TSE2002av refers to the family of devices specified by this document.

The purpose is to provide a standard for the TSE2002av SPD + TS devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTES:

The designation TSE2002av refers to the part of the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

Legacy terminology "master" and "slave" are replaced with "controller" and "target", respectively.

### 2. DEVICE STANDARD

### 2.1 Description

The TSE2002av is a combination 256-byte EEPROM and Temperature Sensor device designed to operate in one of three voltage ranges, 1.7-3.6 V, 2.3-3.6 V, or 3.0-3.6 V. All devices meet the thermal performance characteristics, and the 2.3-3.6 V or 3.0-3.3 V nominal devices shall operate the $I^2C$ bus at a 400 kHz maximum. Both devices are intended to interface to $I^2C$ buses which have multiple devices on a shared bus, and must be uniquely addressed on this bus. A substantial reduction in supply current may be achieved using the software programmed shutdown mode. The device family contains two temperature grades designated with a second letter appended to the part number.

Common Features summary:

| TSE2002av Variations | | | | | | |
|---|---|---|---|---|---|---|
| **Base Part Mumber** | | **a** | **Sensor Accuracy** | | **v** | **Single Supply Voltage** |
| TSE2002 | | B | 0.5 °C typ from 75-95 °C | | 1 | 1.7 to 3.6 V |
| | | | 1.0 °C typ from 40-125 °C | | 2 | 2.3 to 3.6 V |
| | | | 2.0 °C typ from -20-125 °C | | 3 | 3.0 to 3.6 V |
| | | C | 1.0 °C typ from 75-95 °C | | | |
| | | | 2.0 °C typ from 40-125 °C | | | |
| | | | 3.0 °C typ from -20-125 °C | | | |
| Example:   TSE2002C2 is an SPD with Thermal Sensor having 1.0 °C typical accuracy from 75-95 °C and a single supply voltage range from 2.3 to 3.6 V. | | | | | | |

## 2.1 Description (cont'd)

- Low operating current:
  < 100 uA maximum with SPD in Standby and TS in Shutdown mode
  ~1 mA typical with SPD in Standby mode and TS active
  ~2 mA typical with TS and SPD enabled at 3.3 V input
- Two Wire I²C Serial Interface
- Up to 100 kHz Transfer Rate below 2.2 V
- Up to 400 kHz Transfer Rate at or above 2.2 V
- Packages: TSSOP-8, Thermally Enhanced TSSOP-8 (MO-187), PSON-8, SOIC-8, MSOP-8

### SPD Features summary:

- Permanent and Reversible Software Data Protection for Lower 128 Bytes
- Byte and Page (up to 16 Bytes) Write Operation
- Random and Sequential Read modes
- Self-Timed Write Cycle
- Schmitt trigger on bus inputs
- Noise filter on bus inputs
- Automatic Address Incrementing

### TS Features summary:

- Typical accuracy of 1.0 °C accuracy for the active range from 70 ~ 95 °C
- Typical accuracy of 2.0 °C for other monitor ranges from 40 ~ 125 °C
- Support for higher accuracy of 0.5 °C (typical) over the active range, where available
- Ambient temperature (TA) sense through an operating range of -20 to +125 °C
- Temperature sample rate minimum of 8 samples/s
- Selectable 0, 1.5 °C, 3 °C, 6 °C Hysteresis on set point

The SPD section of the TSE2002av is a 2 Kbit serial EEPROM organized as a 256 byte memory. The device is able to lock permanently the data in the lower sector (from location 0x00 to 0x7F), designed specifically for use in DRAM DIMMs (Dual Inline Memory Modules) with Serial Presence Detect. All the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write protected in the first half of the memory.

Locking the lower sector of the SPD may be accomplished using one of two software write protection mechanisms. By sending the device a specific I²C sequence, the first 128 bytes of the memory become write protected, either permanently or resetable.

The TS section of the TSE2002av continuously monitors the temperature and updates the temperature data minimum of eight times per second. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

Internal registers are used to configure both the TS performance and response to over-temperature conditions. The device contains programmable high, low, and critical temperature limits. Finally, the device EVENT# pin can be configured as active high or active low and can be configured to operate as an interrupt or as a comparator output.
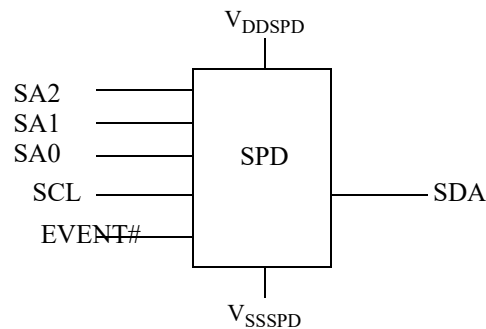
**TS Features Summary (cont'd)**



**Figure 1 — Device Diagram**

## 2.2 Device Interface

The TSE2002av behaves as a target device in the $I^2C$ protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus controller. The START condition is followed by a Device Select Code and R/W# bit (as described in Table 2 on page 6), terminated by an acknowledge bit. TSE2002av family devices shall not initiate clock stretching, which is an optional $I^2C$ bus feature.

In accordance with the $I^2C$ bus definition, the device uses three (3) built-in, 4-bit Device Type Identifier Codes (DTIC) and the state of SA0, SA1, and SA2 to generate an $I^2C$ Target Address. The SPD memory may be accessed using a DTIC of (1010), and to perform the PSWP,CSWP, or PSWP operations a DTIC of (0110) is required. The TS registers are accessed using a DTIC of (0011).

When writing data to the memory, the SPD inserts an acknowledge bit during the 9th bit time, following the bus controller's 8-bit transmission. When data is read by the bus controller, the bus controller acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Bus Controller generated STOP condition after an Ack for WRITE, and after a NoAck for READ.

The TS section of the device uses a pointer register to access all registers in the device. Additionally, all data transfers to and from this section of the device are performed as block read/write operations. The data is transmitted/received as 2 bytes, Most Significant Byte (MSB) first, and terminated with a NoAck and STOP after the Least Significant byte (LSB). Data and address information is transmitted and received Most Significant Bit first
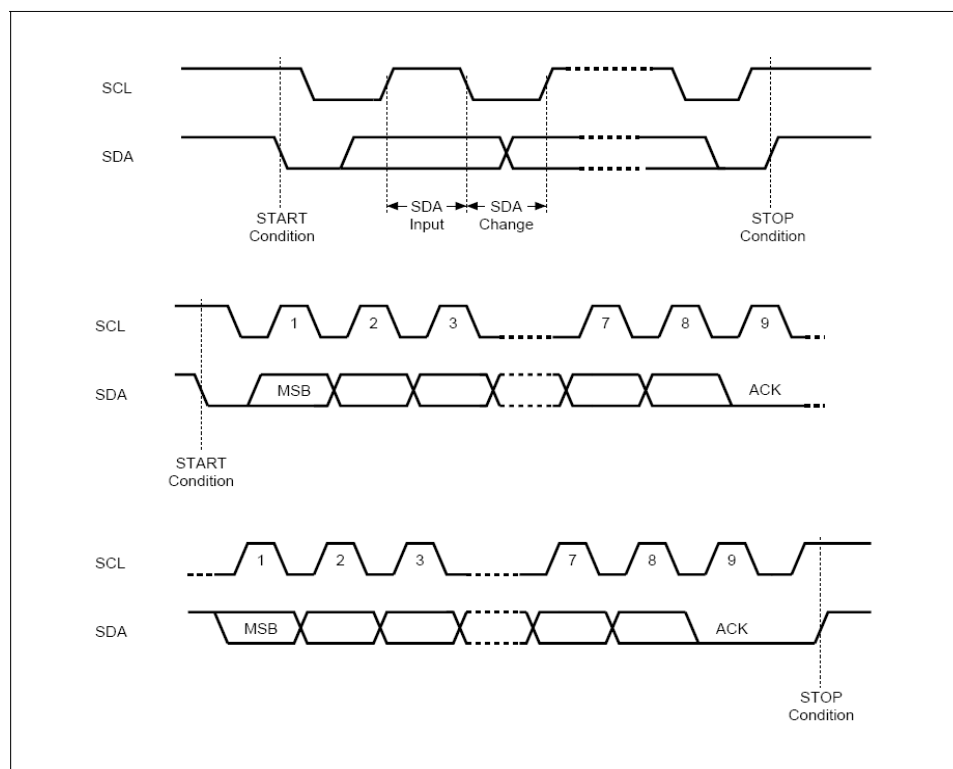
## 2.2 Device Interface (cont'd)



Figure 2 — I²C Bus Protocol

**Start Condition**

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

**Stop Condition**

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus controller. A Read command that is followed by NoAck can be followed by a Stop condition to force the SPD into Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle for the SPD. Neither of these conditions changes the operation of the TS section.

**Acknowledge Bit (ACK)**

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus controller or target device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

**No Acknowledge Bit (NACK)**

The no-acknowledge bit is used to indicate the completion of a block read operation, or an attempt to modify a write-protected register. The bus controller releases Serial Data (SDA) after sending eight bits of data, and during the 9th clock pulse period, and does not pull Serial Data (SDA) Low.

**Data Input**

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change only when Serial Clock (SCL) is driven Low.

**Memory Addressing**

To start communication between the bus controller and the target device, the bus controller must initiate a Start condition. Following this, the bus controller sends the Device Select Code, shown in Table 1 on page 5 (on Serial Data (SDA), most significant bit first).

**Table 1 — Device Select Code**

| Memory Area Function | Device Type Identifier | | | | Select Address Signals | | | R/W# | SA0 Pin |
|---|---|---|---|---|---|---|---|---|---|
| | b7[1] | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
| Read/Write SPD memory | 1 | 0 | 1 | 0 | SA2 | SA1 | SA0 | R/W# | 0 or 1 |
| Set Reversible Write Protection (SWP) | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | $V_{HV}$ |
| Clear Reversible Write Protection (CWP) | | | | | 0 | 1 | 1 | 0 | $V_{HV}$ |
| Read Reversible Write Protection Status | | | | | 0 | 0 | 1 | 1 | $V_{HV}$ |
| Permanently Set Write Protection (PSWP)[2] | | | | | SA2 | SA1 | SA0 | 0 | 0 or 1 |
| Read Permanent Write Protection Status[2] | | | | | SA2 | SA1 | SA0 | 1 | 0 or 1 |
| Read/Write Temperature registers | 0 | 0 | 1 | 1 | SA2 | SA1 | SA0 | R/W# | 0 or 1 |
| Note 1　The most significant bit, b7, is sent first.　Note 2　SA0, SA1, and SA2 are compared against the respective external pins on the TSE2002av.　Note 3　$0 = V_{SSSPD}$, $1 = V_{DDSPD}$, $V_{HV}$ = High Voltage. | | | | | | | | | |

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Select Address (SA2, SA1, SA0). To address the memory array, the 4-bit Device Type Identifier is 1010b; to access the write-protection settings, it is 0110b; and to access the Temperature Sensor settings is 0011b. Additionally, reading or writing the reversible write protect requires that SA0 be raised to the $V_{HV}$ voltage level; setting the permanent write protect may be done with SA0 at either $V_{SSSPD}$ or $V_{DDSPD}$ levels.

Up to eight memory devices can be connected on a single $I^2C$ bus. Each one is given a unique 3-bit code on the Chip Enable (SA0, SA1, SA2) inputs. When the Device Select Code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (SA0, SA1, SA2) inputs.

The 8th bit is the Read/Write bit (R/W#). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the SPD Device Select code, the SPD section deselects itself from the bus, and goes into Standby mode. The $I^2C$ operating modes are detailed in Table 2 on page 6.

**Release 21**

**Memory Addressing (cont'd)**

**Table 2 —  $I^2C$  Operating Modes**

| Mode | R/W# Bit | Bytes | Initial Sequence |
|---|---|---|---|
| SPD Current Address Read | 1 | 1 | START, Device Select, R/W# = 1 |
| SPD Random Address Read | 0 | 1 | START, Device Select, R/W# = 0, Address |
|  | 1 |  | reSTART, Device Select, R/W# = 1 |
| SPD Sequential Read | 1 | ≥ 1 | Similar to Current or Random Address Read |
| SPD Byte Write | 0 | 1 | START, Device Select, R/W# = 0, data, STOP |
| SPD Page Write | 0 | ≤ 16 | START, Device Select, R/W# = 0, data, STOP |
| TS Write | 0 | 2 | START, Device Select, R/W#=0, pointer, data, STOP |
| TS Read | 1 | 2 | START, Device Select, R/W#=1, pointer, data, STOP |

## 2.3 Device Pin Definition

**Table 3 — Pin Description for TSE2002av**

| Pin # | Pin Name | Definition |
|---|---|---|
| 1 | SA0 | Select Address 0 |
| 2 | SA1 | Select Address 1 |
| 3 | SA2 | Select Address 2 |
| 4 | $V_{SSSPD}$ | Ground |
| 5 | SDA | Serial data |
| 6 | SCL | Serial clock |
| 7 | EVENT# | Temperature Event |
| 8 | $V_{DDSPD}$ | Supply voltage |

## 2.4 Pin Functional Description

**Serial Clock (SCL)**

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by target devices to synchronize the bus to a slower clock, the bus controller must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to $V_{DDSPD}$. (Figure 3 on page 7 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus controller has a push-pull (rather than open drain) output.

## Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to the most positive $V_{DDSPD}$ in the $I^2C$ chain. (Figure 3 on page 7 indicates how the value of the pull-up resistor can be calculated).
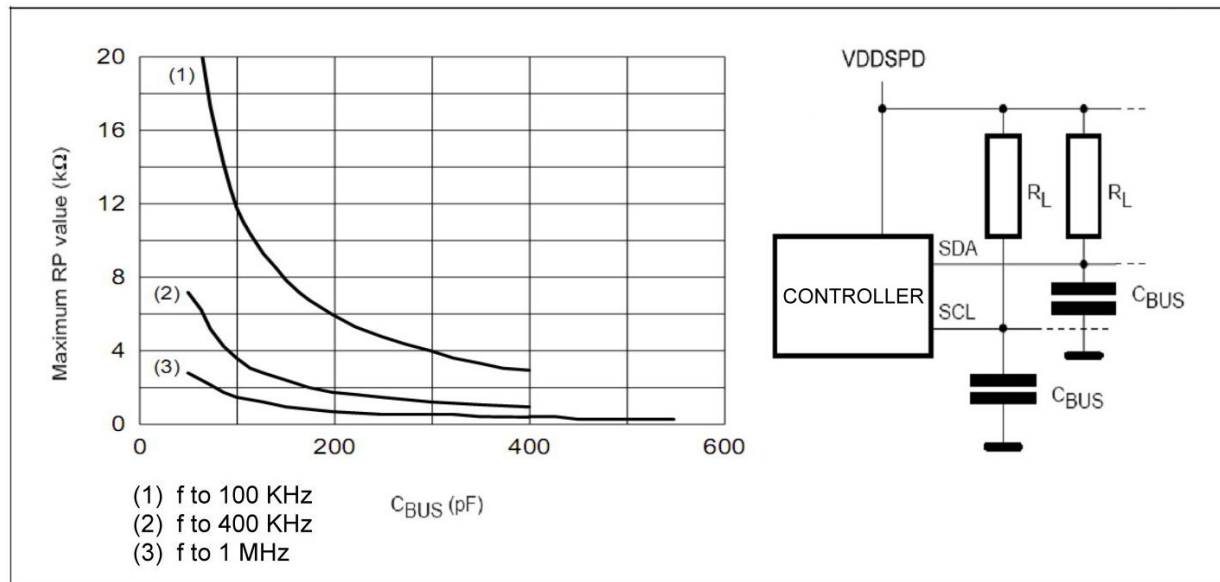


**Figure 3 — Maximum $R_L$ Value Versus Bus Capacitance ($C_{BUS}$) for an $I^2C$ Bus**

## Select Address (SA0, SA1, SA2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Target Address. In the end application, SA0, SA1 and SA2 must be directly (not through a pull-up or pull-down resistor) connected to $V_{DDSPD}$ or $V_{SSSPD}$ to establish the Target Address. When these inputs are not connected, an internal pull-down circuitry makes (SA0, SA1, SA2) = (0, 0, 0).

The SA0 input is used to detect the $V_{HV}$ voltage, when decoding an SWP or CWP instruction. Refer to Table 2 on page 6 for decode details.

## EVENT#

The TSE2002av EVENT# pin is an open drain output that requires a pull-up to $V_{DDSPD}$ on the system motherboard or integrated into the controller. EVENT# has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are Interrupt, Comparator, or TCRIT Only.

In Interrupt Mode, the EVENT# pin will remain asserted until it is released by writing a '1' to the "Clear Event" bit in the Status Register. The value to write is independent of the EVENT# polarity bit.

In Comparator Mode, the EVENT# pin will clear itself when the error condition that caused the pin to be asserted is removed. When the temperature is compared against the TCRIT limit, then this mode is always used.

## EVENT# (cont'd)

Finally, in the TCRIT Only Mode the EVENT# pin will only be asserted if the measured temperature exceeds the TCRIT Limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT Limit minus the TCRIT hysteresis. Figure 4 on page 8 illustrates the operation of the different modes over time and temperature.
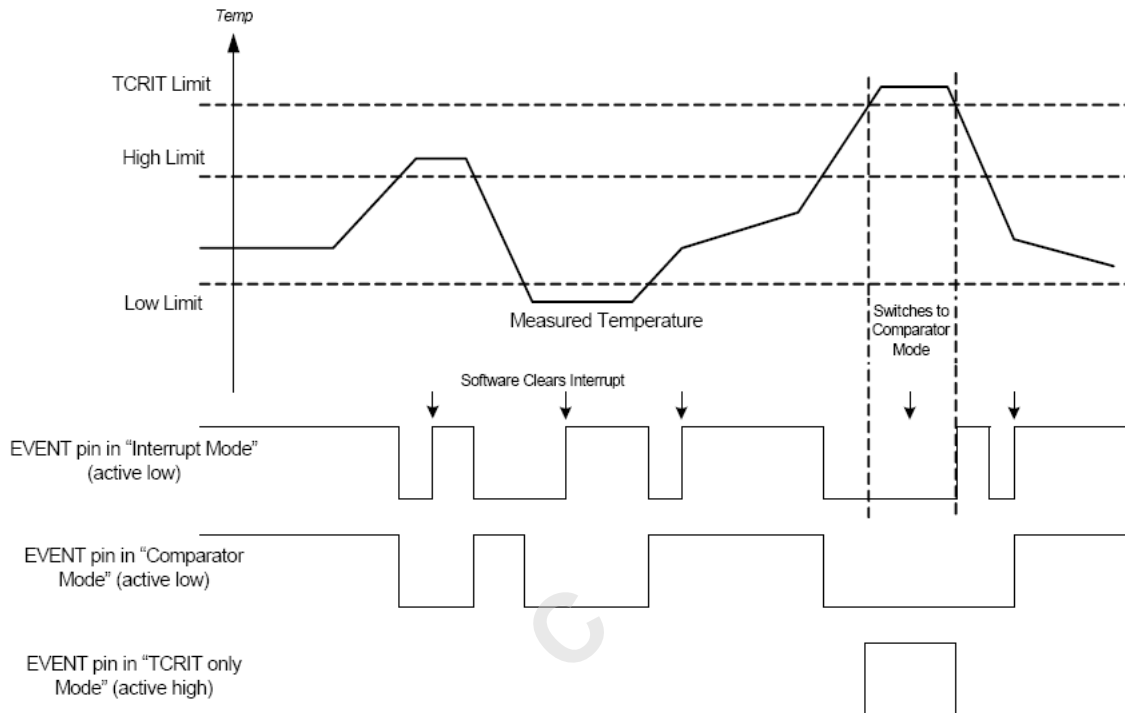


**Figure 4 — EVENT# Pin Mode Functionality**

Systems that use the active high mode for EVENT# must be wired point to point between the TSE2002av and the sensing controller. Wire-OR configurations should not be used with active high EVENT# since any device pulling the EVENT# signal low will mask the other devices on the bus. Also note that the normal state of EVENT# in active high mode is a 0 which will constantly draw power through the pull-up resistor.

## 2.5 Device Reset and Initialization

In order to prevent inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included.

At Power-up (phase during which $V_{DDSPD}$ is lower than $V_{DDSPD}$min but increases continuously), the device will not respond to any instruction until $V_{DDSPD}$ has reached the Power On Reset threshold voltage (this threshold is lower than the minimum $V_{DDSPD}$ operating voltage defined in the DC AND AC PARAMETERS tables). Once $V_{DDSPD}$ has passed the POR threshold, the device is reset. The actual POR threshold voltage will be implementation dependent, and is not defined in this document.

The device is delivered with all bits in the EEPROM memory array set to '1' (each byte contains 0xFF).

Prior to selecting the memory and issuing instructions, a valid and stable $V_{DDSPD}$ voltage must be applied. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle ($t_W$).

## 2.5 Device Reset and Initialization (cont'd)

At Power-down (phase during which $V_{DDSPD}$ decreases continuously), as soon as $V_{DDSPD}$ drops from the normal operating voltage below the minimum operating voltage, the device stops responding to commands, and remains in reset until the POR threshold voltage is reached.

## 2.6 Software Write Protect

The TSE2002av has three software write-protection features, allowing the bottom half of the memory area (addresses 0x00 to 0x7F) to be temporarily or permanently write protected.

Software write-protection is handled by three instructions:

- SWP: Set Write Protection
- CWP: Clear Write Protection
- PSWP: Permanently Set Write Protection

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.
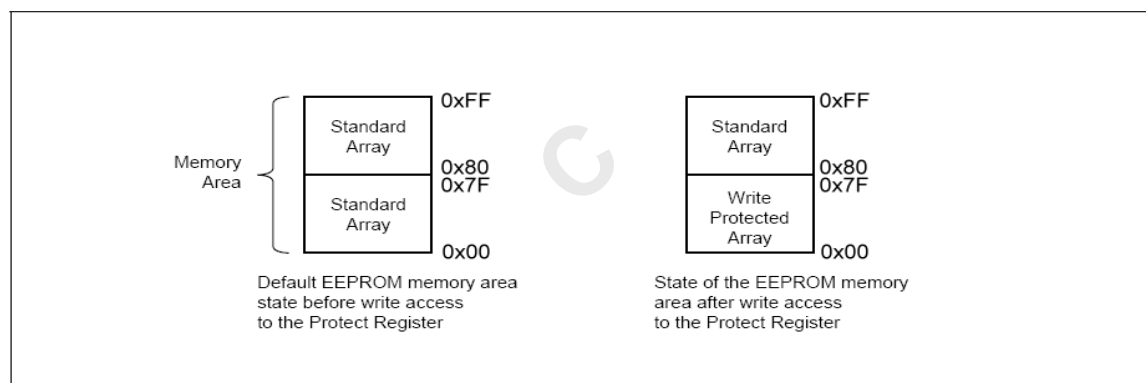


**Figure 5 — Result of Setting the Write Protection**

### SWP and CWP

If the software write-protection has been set with the SWP instruction, it can be cleared again with a CWP instruction.

The two instructions (SWP and CWP) have the same format as a Byte Write instruction, but with a different Device Type Identifier (as shown in Table 2 on page 6). Like the Byte Write instruction, it is followed by an address byte and a data byte, but in this case the contents are all "Don't Care" (Figure 6 on page 10). Another difference is that the voltage, $V_{HV}$, must be applied on the SA0 pin, and specific logical levels must be applied on the other two (SA1 and SA2, as shown in Table 2 on page 6).

### PSWP

If the software write-protection has been set with the PSWP instruction, the first 128 bytes of the memory are permanently write-protected. This write-protection cannot be cleared by any instruction, or by power-cycling the device. Also, once the PSWP instruction has been successfully executed, the TSE2002av no longer acknowledges any instruction (with a Device Type Identifier of 0110) to access the write-protection settings.
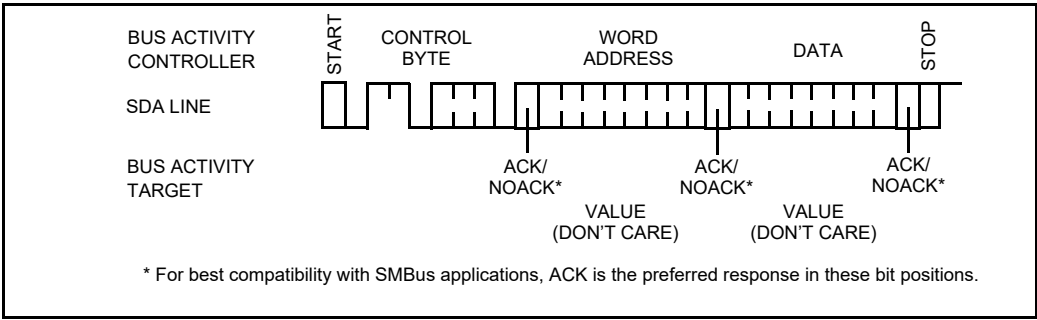
**Release 21**

**PSWP (cont'd)**



**Figure 6 — Setting the Write Protection**

## Reading Write Protection Status

The status of software write protection can be determined using these instructions:

- Read SWP: Read Write Protection Status
- Read PSWP: Read Permanently Set Write Protection Status

## Read SWP

The controller issues a Read SWP command. If Software Write Protection has not been set, the device replies to the data byte with an Ack. If Software Write Protection has been set, the device replies to the data byte with a NoAck.

## Read PSWP

The controller issues a Read PSWP command. If Permanent Software Write Protection has not been set, the device replies to the data byte with an Ack. If Permanent Software Write Protection has been set, the device replies to the data byte with a NoAck.

## 2.7 Write Operations

Following a Start condition the bus controller sends a Device Select Code with the R/W# bit reset to 0. The device acknowledges this, as shown in Table 7 on page 11, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus controller generates a Stop condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored, and the device does not respond to any requests.

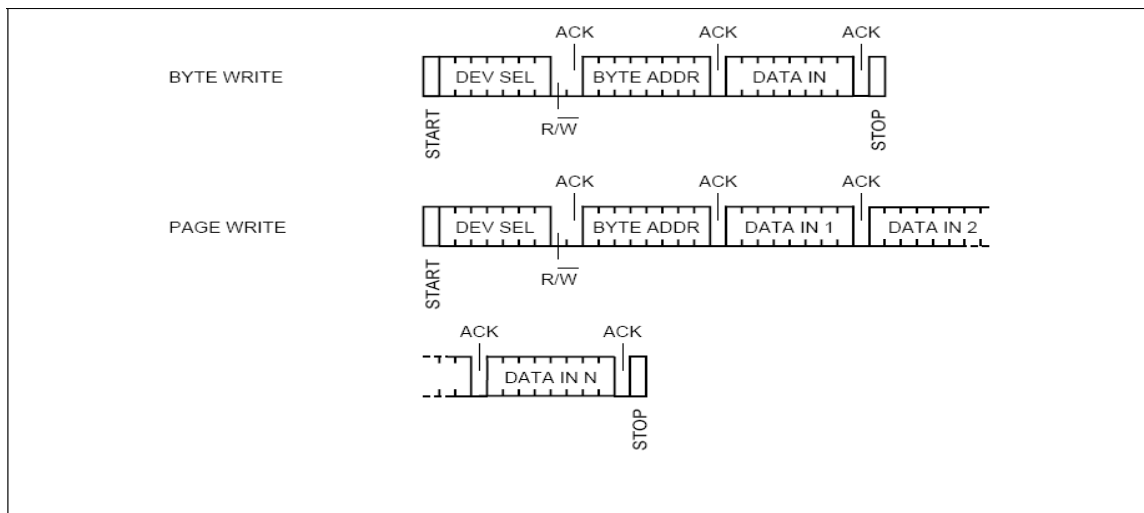**Release 21**

## 2.7 Write Operations (cont'd)



**Figure 7 — Write Mode Sequences in a Non-Write Protected Area**

### Byte Write

After the Device Select Code and the address byte, the bus controller sends one data byte. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus controller terminates the transfer by generating a Stop condition, as shown in Figure 7 on page 11.

### Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as "roll-over" occurs. This should be avoided, as data starts to be over-written in an implementation dependent fashion.

The bus controller sends from 1 to 16 bytes of data, each of which is acknowledged by the device. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter is incremented. The transfer is terminated by the bus controller generating a Stop condition.

## 2.8 Write Cycle Polling Using ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time ($t_W$) is shown in Table 24 on page 29, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus controller.

## 2.8 Write Cycle Polling Using ACK (cont'd)

The sequence, as shown in Figure 8 on page 12, is:

• Initial condition: a Write cycle is in progress.
• Step 1: the bus controller issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
• Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus controller goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).
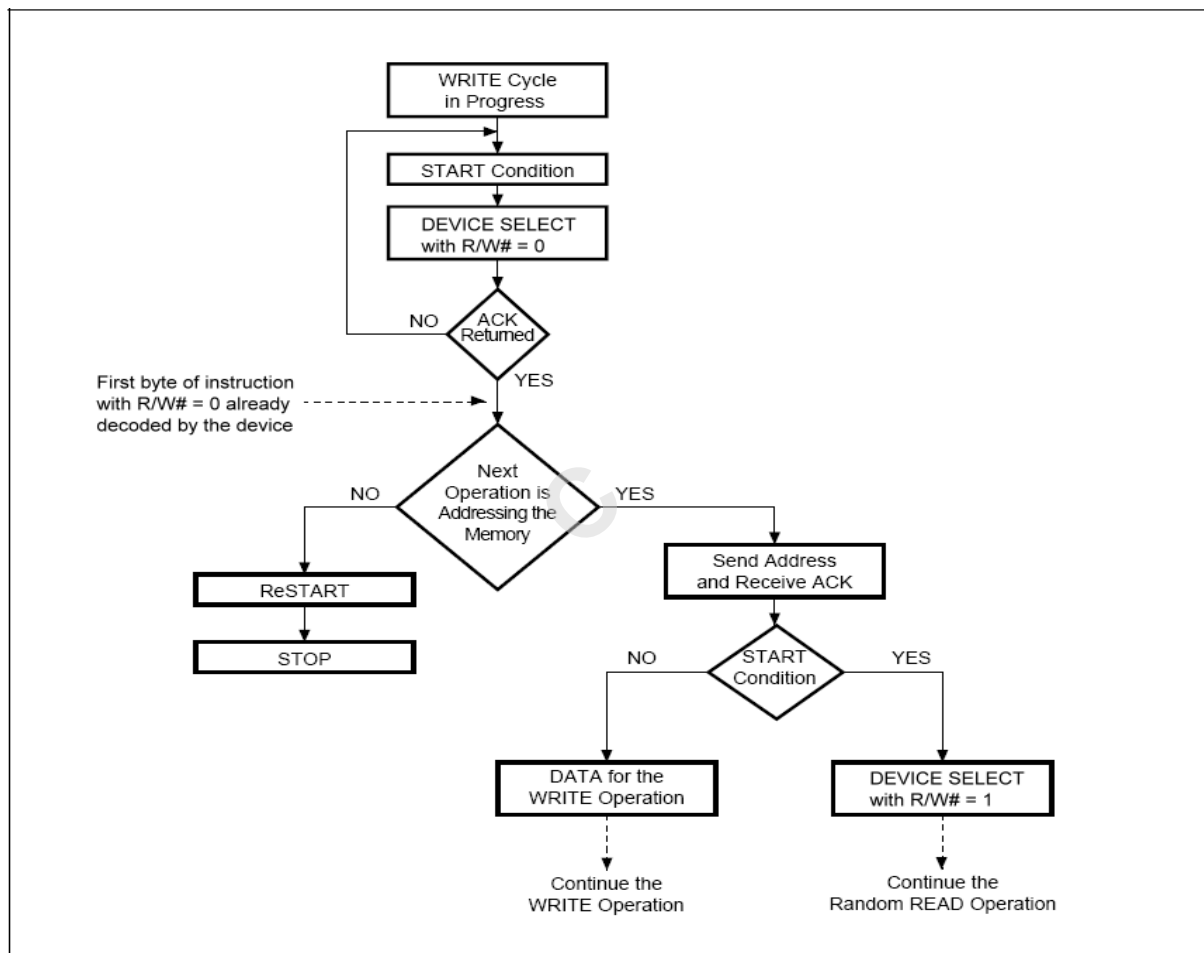


**Figure 8 — Write Cycle Polling FlowChart Using ACK**

## 2.9 Read Operations

Read operations are performed independent of the software protection state.

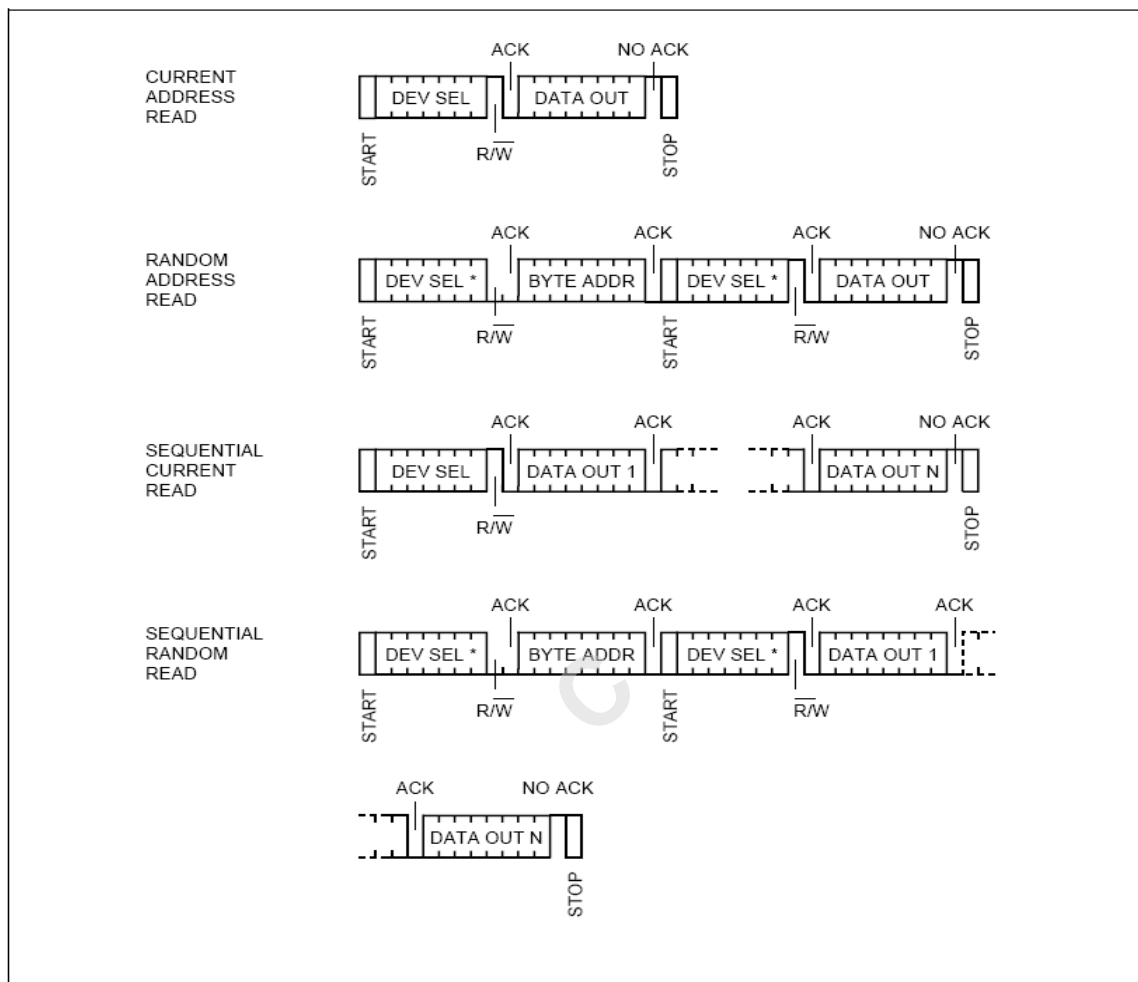The device has an internal address counter which is incremented each time a byte is read.



**Figure 9 — Read Mode Sequences**

**Random Address Read**

A dummy Write is first performed to load the address into this address counter (as shown in Figure 9 on page 13) but without sending a Stop condition. Then, the bus controller sends another Start condition, and repeats the Device Select Code, with the R/W# bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus controller must not acknowledge the byte, and terminates the transfer with a Stop condition.

**Current Address Read**

For the Current Address Read operation, following a Start condition, the bus controller only sends a Device Select Code with the R/W# bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus controller terminates the transfer with a Stop condition, as shown in Figure 9 on page 13, without acknowledging the byte.

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## Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus controller does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus controller must not acknowledge the last byte, and must generate a Stop condition, as shown in Figure 9 on page 13.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 0x00.

## Acknowledge in Read Mode

For all Read commands to the SPD, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus controller does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and returns to an idle state to await the next valid START condition. This has no effect on the TS operational status.

**Table 4 — Acknowledge When Writing Data or Defining Write Protection**
**(Instructions with R/W# bit = 0)**

| Status | Instruction | Ack | Address | Ack | Data byte | Ack | Write Cycle ($t_W$) |
|---|---|---|---|---|---|---|---|
| Permanently protected | PSWP, SWP, or CWP | NoAck | Not significant | NoAck | Not significant | NoAck | No |
| | Page or byte write in lower 128 bytes | Ack | Address | Ack | Data | Ack or NoAck[1] | Yes |
| Protected with SWP | SWP | NoAck | Not significant | NoAck | Not significant | NoAck | No |
| | CWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | PSWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | Page or byte write in lower 128 bytes | Ack | Address | Ack | Data | Ack or NoAck[1] | Yes |
| Not protected | PSWP, SWP, or CWP | Ack | Not significant | Ack | Not significant | Ack | Yes |
| | Page or byte write | Ack | Address | Ack | Data | Ack | Yes |
| NOTE 1    Both implementations exist in the industry. Software must accept either return code. | | | | | | | |

**Table 5 — Acknowledge When Reading the Write Protection**
**(Instructions with R/W# bit = 1)**

| PSWP Status | SWP Status | Instruction | ACK | Address | ACK | Data byte | ACK |
|---|---|---|---|---|---|---|---|
| Set | X | Read PSWP | NoAck | Not significant | NoAck | Not significant | NoAck |
| Not Set | X | Read PSWP | Ack | Not significant | NoAck | Not significant | NoAck |
| Set | X | Read SWP | NoAck | Not significant | NoAck | Not significant | NoAck |
| X | Set | Read SWP | NoAck | Not significant | NoAck | Not significant | NoAck |
| Not Set | Not Set | Read SWP | Ack | Not significant | NoAck | Not significant | NoAck |
| NOTE    X = Set or Not Set. | | | | | | | |

## 2.10 Temperature Sensor (TS) Device Operation

The TSE2002av Temperature Register Set is accessed though the $I^2C$ address 0011_bbb_R/W#. The "bbb" denotes the current state of SA2, SA1, and SA0. In the event SA0 is in the high voltage state, the device shall interpret the voltage as a logic '1' at the pin. The Temperature Register Set stores the temperature data, limits, and configuration values. All registers in the address space from 0x00 through 0x08 are 16-bit registers (see clause 2.12 for detailed information), accessed through block read and write commands.

## 2.11 TS Write Operations

Writing to the TSE2002av Temperature Register Set is accomplished through a modified block write operation for two (2) data bytes. To maintain I2C compatibility, the 16 bit register is accessed through a pointer register, requiring the write sequence to include an address pointer in addition to the Target address. This indicates the storage location for the next two bytes received. Figure 10 shows an entire write transaction on the bus.
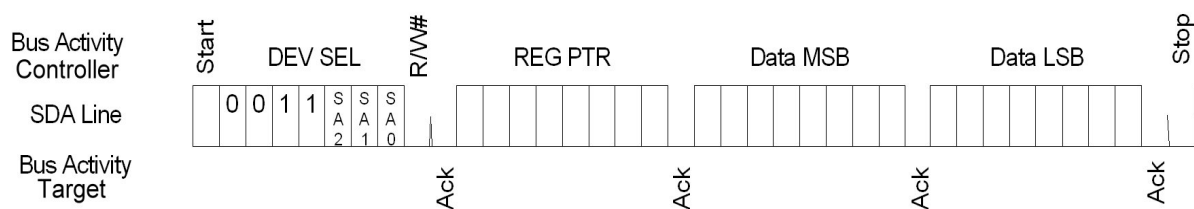


**Figure 10 — TS Register Write Operation**

## 2.12 TS Read Operations

Reading data from the TS may be accomplished in one of two ways:

1. If the location latched in the Pointer Register is correct (for normal operation it is expected the same address will be read repeatedly for temperature), the read sequence may consist of a Target Address from the bus controller followed by two bytes of data from the device; or

2. The pointer register is loaded with the correct register address, and the data is read. The sequence to preset the pointer register is shown in Figure 11, and the preset pointer read is shown in Figure 12. If it is desired to read random address each cycle, the complete Pointer Write, Word Read sequence is shown in Figure 13.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (Ack) or No Acknowledge (No Ack) from the Controller (No Acknowledge is typically used as a signal for the target that the Controller has read its last byte).
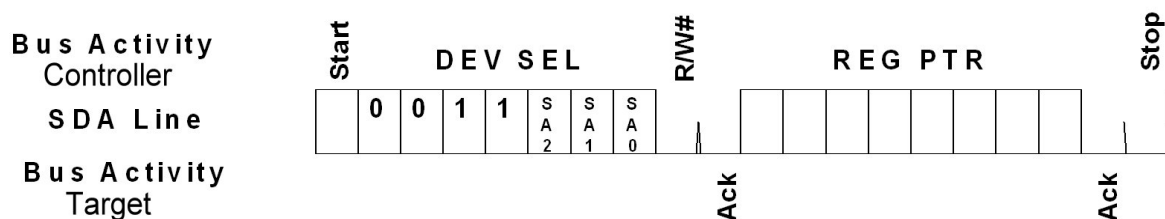


**Figure 11 — $I^2C$ Write to Pointer Register**
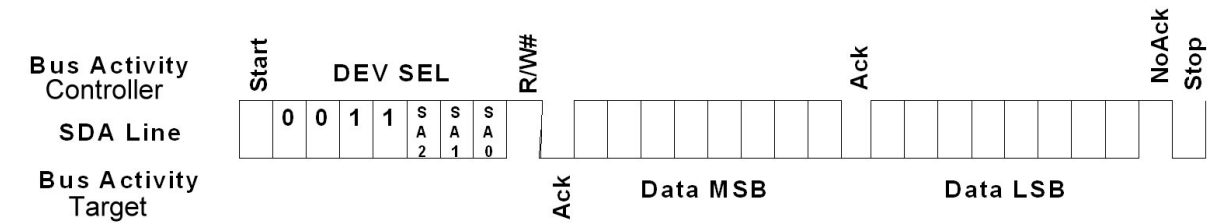
## 2.12 TS Read Operations (cont'd)



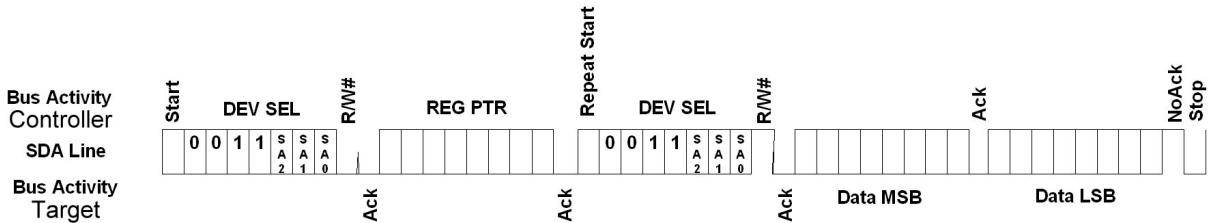**Figure 12 — I$^2$C Preset Pointer Register Word Read**



**Figure 13 — I$^2$C Pointer Write Register Word Read**

## 2.13 TS Register Set Definition

The register set address are shown in Table 4. These values are used in the I$^2$C operations as the "REG_PTR" in Figures 10 through 13.

**Table 6 — Temperature Register Addresses**

| ADDR | R/W | NAME | FUNCTION | DEFAULT |
|---|---|---|---|---|
| N/A | W | Address Pointer | Address storage for subsequent operations | undefined |
| 00 | R | Capabilities | Indicates the functions and capabilities of the temperature sensor | 000F or 002F |
| 01 | R/W | Configuration | Controls the operation of the temperature monitor | 0000 |
| 02 | R/W | High Limit | Temperature High Limit | 0000 |
| 03 | R/W | Low Limit | Temperature Low Limit | 0000 |
| 04 | R/W | TCRIT Limit | Critical Temperature | 0000 |
| 05 | R | Ambient Temperature | Current Ambient temperature | N/A |
| 06 | R | Manufacturer ID | PCI-SIG manufacturer ID | undefined |
| 07 | R | Device/Revision | Device ID and Revision number | 0000 |
| 08-0F | R/W | Vendor-defined | Vendor specific information | 0000 |

## 2.14 Capabilities Register

**Table 7 — Capabilities Register**

| ADDR | R/W | B15 / B7 | B14 / B6 | B13 / B5 | B12 / B4 | B11 / B3 | B10 / B2 | B9 / B1 | B8 / B0 | DEFAULT |
|------|-----|----------|----------|----------|----------|----------|----------|---------|---------|---------|
| 00 | R | RFU | RFU | RFU | RFU | RFU | RFU | RFU | RFU | 000F or 002F |
| | | EVSD | TMOUT | X | TRES[1:0] | | RANGE | ACC | EVENT | |

The Capabilities Register indicates the supported features of the temperature sensor.

Bits 15 - Bit 8 - RFU - Reserved for future use. These bits will always read '0' and writing to them will have no affect

Bit 7 - EVSD - EVENT# with Shutdown action.

'0' (default) - The EVENT# output freezes in its current state when entering shutdown. Upon exiting shutdown, the EVENT# output remains in the previous state until the next thermal sample is taken, or possibly sooner if EVENT# is programmed for comparator mode.

'1' - The EVENT# output is deasserted (not driven) when entering shutdown, and remains deasserted upon exit from shutdown until the next thermal sample is taken, or possibly sooner if EVENT# is programmed for comparator mode.

Bit 6 - TMOUT - Bus timeout period for thermal sensor access during normal operation. Note that bus timeout support is optional in shutdown mode, or for access to the EEPROM portion of the device.

'0' (default) - Parameter $t_{TIMEOUT}$ is supported within the range of 10 to 60 ms.

'1' - Parameter $t_{TIMEOUT}$ is supported within the range of 25 to 35 ms (SMBus compatible).

Bit 5 - X - May be 0 or 1; applications must accept either code. Defined for compatibility with TS3000 devices; since all TSE2002 devices are required to support VHV, this bit is not used.

Bits 4 - 3 - TRES[1:0] - Indicates the resolution of the temperature monitor as shown in Table 8 on page 17

**Table 8 — TRES Bit Decode**

| TRES[1:0] | | TEMPERATURE RESOLUTION |
|-----------|---|------------------------|
| 1 | 0 | |
| 0 | 0 | 0.5 °C (9-bit) |
| 0 | 1 | 0.25 °C (10-bit) (default) |
| 1 | 0 | 0.125 °C (11-bit) |
| 1 | 1 | 0.0625 °C (12-bit) |

## 2.14 Capabilities Register (cont'd)

Bit 2 - RANGE - Indicates the supported temperature range.

'0' - The temperature monitor clamps values lower than 0 °C.

'1' (default) - The temperature monitor can read temperatures below 0 °C and sets the sign bit appropriately.

Bit 1 - ACC - Indicates the supported temperature accuracy.

'0' - The temperature monitor has ±2 °C accuracy of the active range (75 °C to 95 °C) and 3 °C accuracy over the entire operating range.

'1' (default) - The temperature monitor has ±1 °C accuracy over the active range (75 °C to 95 °C) and 2°C accuracy over the monitoring range (40 °C to 125 °C)

Bit 0 - EVENT - Indicates whether the temperature monitor supports interrupt capabilities

'0' - The device does not support interrupt capabilities.

'1' (default) - The device supports interrupt capabilities.

## 2.15 Configuration Register

**Table 9 — Configuration Register**

| ADDR | R/W | B15 / B7 | B14 / B6 | B13 / B5 | B12 / B4 | B11 / B3 | B10 / B2 | B9 / B1 | B8 / B0 | DEFAULT |
|------|-----|----------|----------|----------|----------|----------|----------|---------|---------|---------|
| 01 | R/W | RFU | RFU | RFU | RFU | RFU | HYST[1:0] | | SHDN | 0000 |
| | | TCRIT_LOCK | EVENT_LOCK | CLEAR | EVENT_STS | EVENT_CTRL | TCRIT_ONLY | EVENT_POL | EVENT_MODE | |

The Configuration Register holds the control and status bits of the EVENT# pin as well as general hysteresis on all limits.

Bits 15 - 11 - RFU - Reserved for future use. These bits will always read '0' and writing to them will have no affect. For future compatibility, all RFU bits must be programmed as '0'.

Bits 10 - 9 - HYST[1:0] - Control the hysteresis that is applied to all limits as shown in Table 10 on page 18. This hysteresis applies to all limits when the temperature is dropping below the threshold so that once the temperature is above a given threshold, it must drop below the threshold minus the hysteresis in order to be flagged as an interrupt event. Note that hysteresis is also applied to EVENT# pin functionality. When either of the lock bits is set, these bits cannot be altered.

**Table 10 — HYST Bit Decode**

| HYST[1:0] | | HYSTERESIS |
|---|---|---|
| **1** | **0** | |
| 0 | 0 | disable hysteresis (default) |
| 0 | 1 | 1.5 °C |
| 1 | 0 | 3 °C |
| 1 | 1 | 6 °C |

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## 2.15 Configuration Register (cont'd)

Bit 8 - SHDN - Shutdown. The thermal sensing device and A/D converter are disabled to save power, no events will be generated. When either of the lock bits is set, this bit cannot be set until unlocked. However it can be cleared at any time. When in shutdown mode, TSE2002 devices still respond to commands normally, however bus timeout may or may not be supported in this mode.

> '0' (default) - The thermal sensor is active and converting.

> '1' - The thermal sensor is disabled and will not generate interrupts or update the temperature data.

Bit 7 - TCRIT_LOCK - Locks the TCRIT Limit Register from being updated.

> '0' (default) - The TCRIT Limit Register can be updated normally.

> '1' - The TCRIT Limit Register is locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.

Bit 6 - EVENT_LOCK - Locks the High and Low Limit Registers from being updated.

> '0' (default) - The High and Low Limit Registers can be updated normally.

> '1' - The High and Low Limit Registers are locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.

Bit 5 - CLEAR - Clears the EVENT# pin when it has been asserted. This bit is write only and will always read '0'.

> '0' - does nothing

> '1' - The EVENT# pin is released and will not be asserted until a new interrupt condition occurs. This bit is ignored if the device is operating in Comparator Mode. This bit is self clearing.

Bit 4 - EVENT_STS - Indicates if the EVENT# pin is asserted. This bit is read only.

> '0' (default) - The EVENT# pin is not being asserted by the device.

> '1' - The EVENT# pin is being asserted by the device.

Bit 3 - EVENT_CTRL - Masks the EVENT# pin from generating an interrupt. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

> '0' (default) - The EVENT# pin is disabled and will not generate interrupts.

> '1' - The EVENT# pin is enabled.

Bit 2 - TCRIT_ONLY - Controls whether the EVENT# pin will be asserted from a high / low out-of-limit condition. When the EVENT_LOCK bit is set, this bit cannot be altered.

> '0' (default) - The EVENT# pin will be asserted if the measured temperature is above the High Limit or below the Low Limit in addition to if the temperature is above the TCRIT Limit.

> '1' - The EVENT# pin will only be asserted if the measured temperature is above the TCRIT Limit.

Bit 1 - EVENT_POL - Controls the "active" state of the EVENT# pin. The EVENT# pin is driven to this state when it is asserted. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

> '0' (default) - The EVENT# pin is active low. The "active" state of the pin will be logical '0'.

> '1' - The EVENT# pin is active high. The "active" state of the pin will be logical '1'.

Bit 0 - EVENT_MODE - Controls the behavior of the EVENT# pin. The EVENT# pin may function in either comparator or interrupt mode. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

> '0' - The EVENT# pin will function in comparator mode

> '1' - The EVENT# pin will function in interrupt mode

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**Temperature Register Value Definitions**

Temperatures in the High Limit Register, Low Limit Register, TCRIT Register, and Temperature Data Register are expressed in two's complement format. Bits B12 through B2 for each of these registers are defined for all device resolutions as defined in the TRES field of the Capabilities Register, hence a 0.25 °C minimum granularity is supported in all registers. Examples of valid settings and interpretation of temperature register bits:

| Temperature Register Coding Examples | | |
|---|---|---|
| B15~B0 (binary) | Value | Units |
| xxx0 0000 0010 11xx | +2.75 | °C |
| xxx0 0000 0001 00xx | +1.00 | °C |
| xxx0 0000 0000 01xx | +0.25 | °C |
| xxx0 0000 0000 00xx | 0 | °C |
| xxx1 1111 1111 11xx | -0.25 | °C |
| xxx1 1111 1111 00xx | -1.00 | °C |
| xxx1 1111 1101 01xx | -2.75 | °C |

The TRES field of the Capabilities Register optionally defines higher resolution devices. For compatibility and simplicity, this additional resolution affects only the Temperature Data Register but none of the Limit Registers. When higher resolution devices generate status or EVENT# changes, only bits B12 through B2 are used in the comparison; however, all 11 bits (TRES[1-0] = 10) or all 12 bits (TRES[1-0] = 11) are visible in reads from the Temperature Data Register.

When a lower resolution device is indicated in the Capabilities Register (TRES[1-0] = 00), the finest resolution supported is 0.5 °C. When this is detected, bit 2 of all Limit Registers should be programmed to 0 to assure correct operation of the temperature comparitors.

## 2.16 High Limit Register

The temperature limit registers (High, Low, and TCrit) define the temperatures to be used by various on-chip comparitors to determine device temperature status and thermal EVENTs. For future compatibility, unused bits "-" must be programmed as 0.

**Table 11 — High Limit Register**

| ADDR | R/W | B15 / B7 | B14 / B6 | B13 / B5 | B12 / B4 | B11 / B3 | B10 / B2 | B9 / B1 | B8 / B0 | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|
| 02 | R/W | - | - | - | Sign | 128 | 64 | 32 | 16 | |
| | | 8 | 4 | 2 | 1 | 0.5 | 0.25 | - | - | |

The High Limit Register holds the High Limit for the nominal operating window. When the temperature rises above the High Limit, or drops below or equal to the High Limit, then the EVENT# pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register see Table 9 on page 18), then this register becomes read-only.

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## 2.17 Low Limit Register

**Table 12 — Low Limit Register**

| ADDR | R/W | B15 / B7 | B14 / B6 | B13 / B5 | B12 / B4 | B11 / B3 | B10 / B2 | B9 / B1 | B8 / B0 | DEFAULT |
|------|-----|----------|----------|----------|----------|----------|----------|---------|---------|---------|
| 03 | R/W | - | - | - | Sign | 128 | 64 | 32 | 16 | |
| | | 8 | 4 | 2 | 1 | 0.5 | 0.25 | - | - | |

The Low Limit Register holds the lower limit for the nominal operating window. When the temperature drops below the Low Limit or rises up to meet or exceed the Low Limit, then the EVENT# pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register see Table 9 on page 18), then this register becomes read-only.

## 2.18 TCRIT Limit Register

**Table 13 — TCRIT Limit Register**

| ADDR | R/W | B15 / B7 | B14 / B6 | B13 / B5 | B12 / B4 | B11 / B3 | B10 / B2 | B9 / B1 | B8 / B0 | DEFAULT |
|------|-----|----------|----------|----------|----------|----------|----------|---------|---------|---------|
| 04 | R/W | - | - | - | Sign | 128 | 64 | 32 | 16 | |
| | | 8 | 4 | 2 | 1 | 0.5 | 0.25 | - | - | |

The TCRIT Limit Register holds the TCRIT Limit. If the temperature exceeds the limit, the EVENT# pin will be asserted. It will remain asserted until the temperature drops below or equal to the limit minus hysteresis. If the TCRIT_LOCK bit is set in the Configuration Register (see Table 9 on page 18), then this register becomes read-only.

## 2.19 Temperature Data Register

**Table 14 — Temperature Data Register**

| ADDR | R/W | B15 / B7 | B14 / B6 | B13 / B5 | B12 / B4 | B11 / B3 | B10 / B2 | B9 / B1 | B8 / B0 | DEFAULT |
|------|-----|----------|----------|----------|----------|----------|----------|---------|---------|---------|
| 05 | R | TCRIT | HIGH | LOW | Sign | 128 | 64 | 32 | 16 | N/A (0000) |
| | | 8 | 4 | 2 | 1 | 0.5 | 0.25* | 0.125* | 0.0625* | |

NOTE *   Resolution defined based on value of TRES field of the Capabilties Register.  Unused/unsupported bits will read as 0.

The Temperature Data Register holds the 10-bit + sign data for the internal temperature measurement as well as the status bits indicating which error conditions, if any, are active.  The encoding of bits B12 through B0 is the same as for the temperature limit registers.

Bit 15 - TCRIT - When set, the temperature is above the TCRIT Limit. This bit will remain set so long as the temperature is above TCRIT and will automatically clear once the temperature has dropped below the limit minus the hysteresis.

Bit 14 - HIGH - When set, the temperature is above the High Limit. This bit will remain set so long as the temperature is above the HIGH limit. Once set, it will only be cleared when the temperature drops below or equal to the HIGH Limit minus the hysteresis.

Bit 13 - LOW - When set, the temperature is below the Low Limit. This bit will remain set so long as the temperature is below the Low Limit minus the hysteresis. Once set, it will only be cleared when the temperature meets or exceeds the Low Limit.

## 2.20 Manufacturer ID Register

**Table 15 — Manufacturer ID Register**

| ADDR | R/W | B15 / B7 | B14 / B6 | B13 / B5 | B12 / B4 | B11 / B3 | B10 / B2 | B9 / B1 | B8 / B0 | DEFAULT |
|------|-----|----------|----------|----------|----------|----------|----------|---------|---------|---------|
| 06 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000 |
|  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

The Manufacturer ID Register holds the PCI SIG number assigned to the specific manufacturer.

## 2.21 Device ID / Revision Register

**Table 16 — Device ID / Revision Register**

| ADDR | R/W | B15 / B7 | B14 / B6 | B13 / B5 | B12 / B4 | B11 / B3 | B10 / B2 | B9 / B1 | B8 / B0 | DEFAULT |
|------|-----|----------|----------|----------|----------|----------|----------|---------|---------|---------|
| 07 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000 |
|  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

The upper byte of the Device ID / Revision Register stores a unique number indicating the TSE2002av from other devices. The lower byte holds the revision value.

## 2.22 Use in a Memory Module

In the Dual Inline Memory Module (DIMM) application, the TSE2002av is soldered directly onto the printed circuit module. The three Select Address inputs (SA0, SA1, SA2) must be connected to $v_{SSSPD}$ or $v_{DDSPD}$ directly (that is without using a pull-up or pull-down resistor) through the DIMM socket (see Table 17 on page 23). The pull-up resistors needed for normal behavior of the $I^2C$ bus are connected on the $I^2C$ bus of the motherboard.

**Table 17 — Unique Addressing of SPDs in DIMM Applications**

| DIMM Position | SA2 | SA1 | SA0 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |
| NOTE    $0 = V_{SSSPD}$, $1 = V_{DDSPD}$ | | | |

The EVENT# pin is expected to be used in a wire-OR configuration with a pullup resistor to $V_{DDSPD}$ on the motherboard.  In this configuration, EVENT# should be programmed for the active low mode.  Also note that comparator mode or TCRIT-only mode for EVENT# on a wire-OR bus will show the combined results of all devices wired to the EVENT# signal.

The common landing pattern recommendations for the PSON-8 packaged SPD (EE1002 compatible) or SPD with Thermal Sensor (TSE2002 compatible) are parameterized to allow for routing design constraints.  These apply to the use of devices following MO-229 variations
V/WCED-3 and V/WEED-7.  The preferred implementation with wide corner pads enhances device centering during assembly, but two narrower options are defined for modules with tight routing requirements.  This is included for reference only; please refer to JESD21C-4.1.2 for details.

## 2.22 Use in a Memory Module (cont'd)
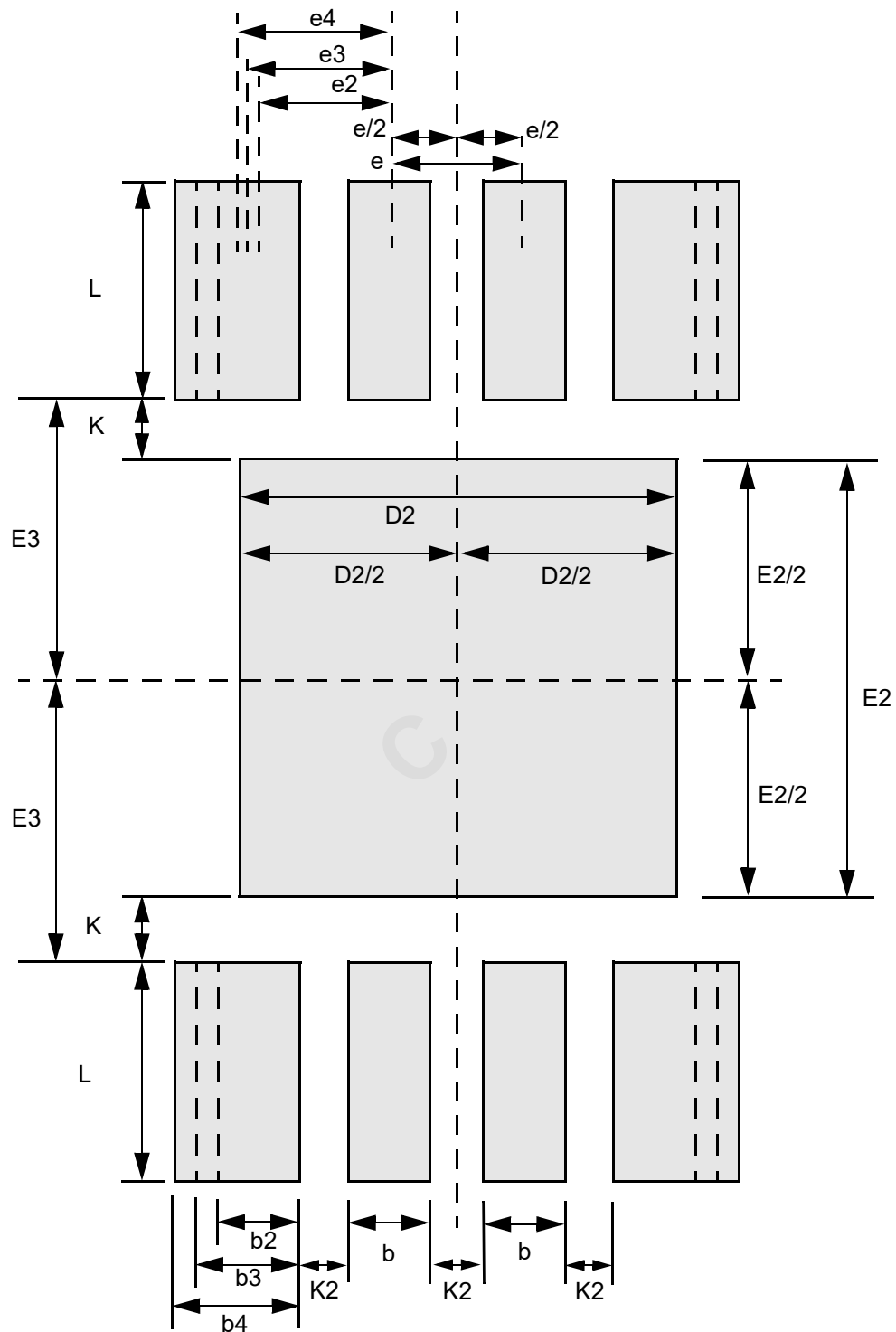
## 2.22 Use in a Memory Module (cont'd)

Table 18 lists three variations of landing pattern implementations, ranked as "Preferred", "Intermediate", and "Minimum Acceptable".

**Table 18 — Parameters for SPD Common Landing Pattern**

| Parameter | Description | Dimension | | | Notes |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| D2 | Heat paddle width | 1.40 | - | 1.60 | |
| E2 | Heat paddle height | 1.40 | - | 1.60 | |
| E3 | Heat paddle centerline to contact inner locus | 1.00 | - | 1.05 | |
| L | Contact length | 0.70 | - | 0.80 | |
| K | Heat paddle to contact keepout | 0.20 | - | - | |
| K2 | Contact to contact keepout | 0.20 | - | - | |
| e | Contact centerline to contact centerline pitch for inner contacts | - | 0.50 | - | |
| b | Contact width for inner contacts | 0.25 | - | 0.30 | |
| e2 | Landing pattern centerline to outer contact centerline, "minimum acceptable" option | - | 0.50 | - | 1 |
| b2 | Corner contact width, "minimum acceptable" option | 0.25 | - | 0.30 | 1 |
| e3 | Inner contact centerline to outer contact centerline, "intermediate" option | - | 0.55 | - | 2 |
| b3 | Corner contact width, "intermediate" option | 0.35 | - | 0.40 | 2 |
| e4 | Landing pattern centerline to outer contact centerline, "preferred" option | - | 0.60 | - | 3 |
| b4 | Corner contact width, "preferred" option | 0.45 | - | 0.50 | 3 |
| NOTE 1   Minimum acceptable option to be used when routing prevents preferred or intermediate width contact. | | | | | |
| NOTE 2   Intermediate option to be used when routing prevents preferred width contact. | | | | | |
| NOTE 3   Preferred option to be used when possible. | | | | | |

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## 2.23 Programming the TSE2002av

The situations in which the TSE2002av is programmed can be considered under two headings:

- when the DIMM is isolated (not inserted on the PCB motherboard)
- when the DIMM is inserted on the PCB motherboard

### DIMM Isolated

With specific programming equipment, it is possible to define the TSE2002av content, using Byte and Page Write instructions, and its write-protection using the SWP and CWP instructions. To issue the SWP and CWP instructions, the DIMM must be inserted in the application-specific slot where the SA0 signal can be driven to $V_{HV}$ during the whole instruction. This programming step is mainly intended for use by DIMM makers, whose end application manufacturers will want to clear this write-protection with the CWP on their own specific programming equipment, to modify the lower 128 Bytes, and finally to set permanently the write-protection with the PSWP instruction.

### DIMM Inserted in the Application Mother Board

As the final application cannot drive the SA0 pin to $V_{HV}$, the only possible action is to freeze the write-protection with the PSWP instruction.Table 4 on page 14 and Table 5 on page 14 show how the Ack bits can be used to identify the write-protection status.

## 2.24 Maximum Ratings

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating clauses of this standard is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 19 — Absolute Maximum Ratings for TSE2002av**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | -65 | 150 | °C |
| $V_{IO}$ | Input or output range, SA0 | -0.50 | 10.0 | V |
| | Input or output range, other pins | -0.50 | 4.3 | V |
| $V_{DDSPD}$ | Supply voltage | -0.5 | 4.3 | V |

## 2.25 DC and AC Parameters

This clause summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

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## 2.25  DC and AC Parameters (cont'd)

**Table 20 — Operating Conditions for TSE2002av family**

| Symbol | Parameter | TSE2002a1 | | TSE2002a2 | | TSE2002a3 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $V_{DDSPD}$ | Supply Voltage | 1.7 | 3.6 | 2.3 | 3.6 | 3.0 | 3.6 | V |
| $T_C$ | Case operating temperature | 0 | 95 | 0 | 95 | 0 | 95 | °C |

**Table 21 — AC Measurement Conditions for TSE2002av**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $C_L$ | Load capacitance | 100 | | pF |
| | Input rise and fall times | -- | 50 | ns |
| | Input levels | $0.2 * V_{DDSPD}$ to $0.8 * V_{DDSPD}$ | | V |
| | Input and output timing reference levels | $0.3 * V_{DDSPD}$ to $0.7 * V_{DDSPD}$ | | V |

**Input levels**

**Input and output timing reference levels**

$0.8 * V_{DDSPD}$

$0.7 * V_{DDSPD}$
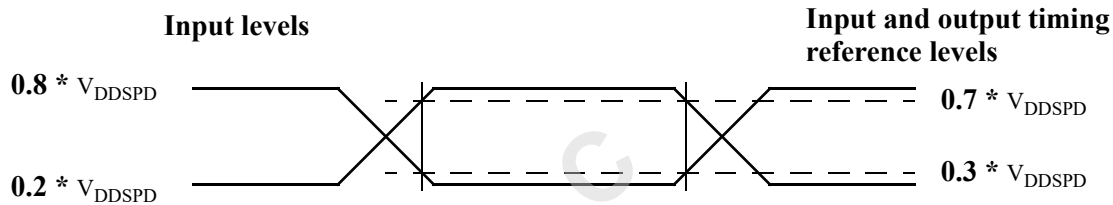
$0.2 * V_{DDSPD}$

$0.3 * V_{DDSPD}$

**Figure 14 — AC Measurement I/O Waveform**

**Table 22 — Input Parameters for TSE2002av**

| Symbol | Parameter[1,2] | Test Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance (SDA) | -- | -- | 8 | pF |
| $C_{IN}$ | Input capacitance (other pins) | -- | -- | 6 | pF |
| $Z_{EIL}$ | Ei (SA0, SA1, SA2) input impedance | $V_{IN} < 0.3 * V_{DDSPD}$ | 30 | -- | kΩ |
| $Z_{EIH}$ | Ei (SA0, SA1, SA2) input impedance | $V_{IN} > 0.7 * V_{DDSPD}$ | 800 | -- | kΩ |
| $t_{SP}$ | Pulse width of spikes which must be suppressed by the input filter | Single glitch, $f \leq 100$ KHz | -- | -- | ns |
| | | Single glitch, $f > 100$ KHz | 0 | 50 | |
| NOTE 1    TA = 25 °C, f = 400 kHz. | | | | | |
| NOTE 2    Verified by design and characterization, not necessarily tested on all devices. | | | | | |

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## 2.25  DC and AC Parameters (cont'd)

DC Characteristics are listed separately for the wide voltage range TSE2002av.

**Table 23 — DC Characteristics for TSE2002av**

| Symbol | Parameter | Test Condition (in addition to those in Table 20 on page 27) | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input leakage current (SCL, SDA) | $V_{IN} = V_{SSSPD}$ or $V_{DDSPD}$ | -- | $\pm 5$ | µA |
| $I_{LO}$ | Output leakage current | $V_{OUT} = V_{SSSPD}$ or $V_{DDSPD}$, SDA in Hi-Z | -- | $\pm 5$ | µA |
| $I_{DD}$ | Supply current | $V_{DDSPD} = 3.3$ V, $f_C = 100$ kHz (rise/fall time < 30 ns) | -- | 2 | mA |
| $I_{DD1}$ | Standby Supply current | $V_{IN} = V_{SSSPD}$ or $V_{DDSPD}$, $V_{DDSPD} = 3.6$ V | -- | 100 | µA |
| | | $V_{IN} = V_{SSSPD}$ or $V_{DDSPD}$, $V_{DDSPD} = 1.7$ V | -- | 100 | µA |
| $V_{IL}$ | Input low voltage (SCL, SDA) | -- | -0.5 | $0.3 * V_{DDSPD}$ | V |
| $V_{IH}$ | Input high voltage (SCL, SDA) | -- | $0.7 * V_{DDSPD}$ | $V_{DDSPD} + 1$ | V |
| $V_{HV}$ | SA0 high voltage | $V_{HV} - V_{DDSPD} \geq 4.8$ V | 7 | 10 | V |
| $V_{OL}$ | Output low voltage | IOL = 2.1 mA, $2.3$ V $\leq V_{DDSPD} \leq 3.6$ V | -- | 0.4 | V |
| | | IOL = 0.7 mA, $V_{DDSPD} = 1.7 - 3.6$V | -- | 0.2 | V |
| $V_{HYST}$[1] | Input hysteresis | $V_{DDSPD} < 2.2$V | $0.10 * V_{DDSPD}$ | -- | V |
| | | $V_{DDSPD} \geq 2.2$V | $0.05 * V_{DDSPD}$ | -- | V |
| NOTE 1   Optional. | | | | | |

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## 2.25  DC and AC Parameters (cont'd)

### Table 24 — AC Characteristics for TSE2002av

| Symbol | Parameter | $V_{DDSPD} < 2.2\ V$[4] | | $V_{DDSPD} \geq 2.2\ V$ | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{SCL}$ | Clock frequency | 10 | 100 | 10 | 400 | kHz |
| $t_{HIGH}$ | Clock pulse width high time | 4000 | -- | 600 | -- | ns |
| $t_{LOW}$[6] | Clock pulse width low time | 4700 | -- | 1300 | -- | ns |
| $t_{TIMEOUT}$[9] | Detect clock low timeout, Capabilities Register bit 6 = 0 | 10 | 60 | 10 | 60 | ms |
| $t_{TIMEOUT}$[9] | Detect clock low timeout, Capabilities Register bit 6 = 1 | 25 | 35 | 25 | 35 | ms |
| $t_R$[2] | SDA rise time | -- | 1000 | 20 | 300 | ns |
| $t_F$[2] | SDA fall time | -- | 300 | 20 | 300 | ns |
| $t_{SU:DAT}$ | Data in setup time | 250 | -- | 100 | -- | ns |
| $t_{HD:DI}$ | Data in hold time | 0 | -- | 0 | -- | ns |
| $t_{HD:DAT}$[5] | Data out hold time | 200 | 3450 | 200 | 900 | ns |
| $t_{SU:STA}$[1] | Start condition setup time | 4700 | -- | 600 | -- | ns |
| $t_{HD:STA}$ | Start condition hold time | 4000 | -- | 600 | -- | ns |
| $t_{SU:STO}$ | Stop condition setup time | 4000 | -- | 600 | -- | ns |
| $t_{BUF}$ | Time between Stop Condition and next Start Condition | 4700 | -- | 1300 | -- | ns |
| $t_W$ | Write time | -- | 10 | -- | 10 | ms |

NOTE 1   For a reSTART condition, or following a write cycle.
NOTE 2   Guaranteed by design and characterization, not necessarily tested.
NOTE 3   To avoid spurious START and STOP conditions, a minimum delay is placed between falling edge of SCL and the falling or rising edge of SDA
NOTE 4   $V_{DDSPD}$ below 2.2 V only supported on TSE2002a1, not on TSE2002a2 or TSE2002a3.
NOTE 5   This specification may conflict with SMBus timing specifications.
NOTE 6   TSE2002av family devices shall not initiate clock stretching, which is an optional $I^2C$ bus feature.
   NOTE 7   Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT,MIN}$. After the controller in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. Typical device examples include the host controller, and embedded controller and most devices that can control the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition.  A timeout condition can only be ensured if the device that is forcing the timeout holds SCL low for $t_{TIMEOUT,MAX}$ or longer.
NOTE 8   TSE2002av family devices are not required to support the SMBus ALERT function.
NOTE 9   Bus timeout value supported depends on setting of TMOUT bit 6 in the Capabilities Register.

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## 2.25 DC and AC Parameters (cont'd)

**Table 25 — Temperature-to-Digital Conversion Performance**

| Parameter | Min | Typ | Max | Unit | Test Conditions[3] |
|---|---|---|---|---|---|
| Temperature Sensor Accuracy (C grade)[1] | -- | ±1.0 | ±2.0 | °C | 75 °C = $T_A$ = 95 °C, Active Range |
|  | -- | ±2.0 | ±3.0 | °C | 40 °C = $T_A$ = 125 °C, Monitor Range |
|  | -- | ±3.0 | ±4.0 | °C | -20 °C = $T_A$ = 125 °C |
| Temperature Sensor Accuracy (B grade)[1] | -- | ±0.5 | ±1.0 | °C | 75 °C = $T_A$ = 95 °C, Active Range |
|  | -- | ±1.0 | ±2.0 | °C | 40 °C = $T_A$ = 125 °C, Monitor Range |
|  | -- | ±2.0 | ±3.0 | °C | -20 °C = $T_A$ = 125 °C |
| Resolution |  | 0.25 |  | °C |  |
| Conversion Time[2] |  |  | 125 | ms | Worst case conversion time |
| NOTE 1 | Refer to individual vendor datasheets for explanation of accuracy testing methodology. |||||
| NOTE 2 | Assuming 10-bit resolution.  Conversion times may range from 62.5 ms for 9-bit to 500 ms for 12-bit accuracy. |||||
| NOTE 3 | $V_{DDSPDMIN} \leq V_{DDSPD} \leq V_{DDSPDMAX}$. |||||



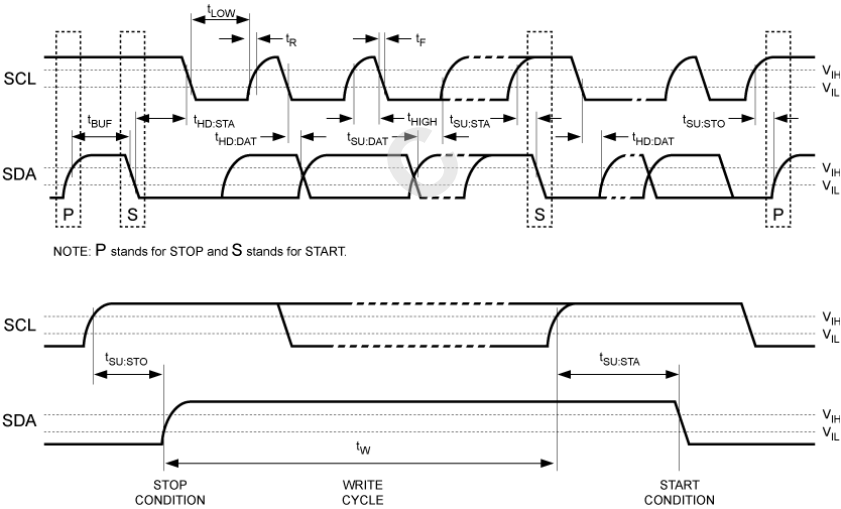NOTE: P stands for STOP and S stands for START.

**Figure 15 — AC Waveforms**

## 3. PACKAGING OPTIONS

**PSON-8:   8-lead Plastic Small Outline No Lead Package Outline**

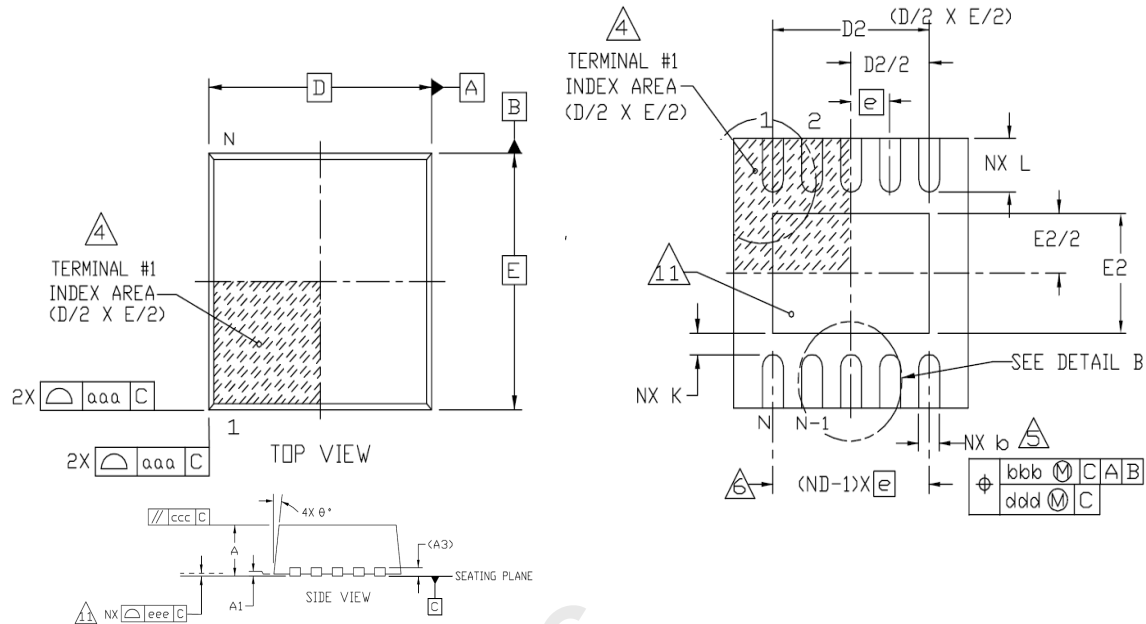**(MO-229; 2x3 mm = Variation V/WCED-3, 3x3 mm = Variation V/WEED-7)**



**Figure 16 — PSON-8 Package Outline**

**Table 26 — PSON-8 Critical Package Dimensions**

| Symbol | Min | Typ | Max | Units | Notes |
|--------|-----|-----|-----|-------|-------|
| A | >0.80 | 0.90 | 1.00 | mm | Var. V |
| A | 0.70 | 0.75 | 0.80 | mm | Var. W |
| D | -- | 2.00 | -- | mm | Basic, Var. V/WCED-3 |
| D | -- | 3.00 | -- | mm | Basic, Var. V/WEED-7 |
| D2 | 1.20 | -- | 1.60 | mm | |
| E | -- | 3.00 | -- | mm | Basic |
| E2 | 1.20 | -- | 1.60 | mm | |
| L | 0.30 | -- | 0.45 | mm | |
| K | 0.20 | -- | -- | mm | |
| N | | 8 | | Leads | |

Device Pinout

| | | | |
|------|---|---|--------|
| SA0 | 1 | 8 | $V_{DDSPD}$ |
| SA1 | 2 | 7 | EVENT# |
| SA2 | 3 | 6 | SCL |
| $V_{SSSPD}$ | 4 | 5 | SDA |

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## 3.  PACKAGING OPTIONS (cont'd)
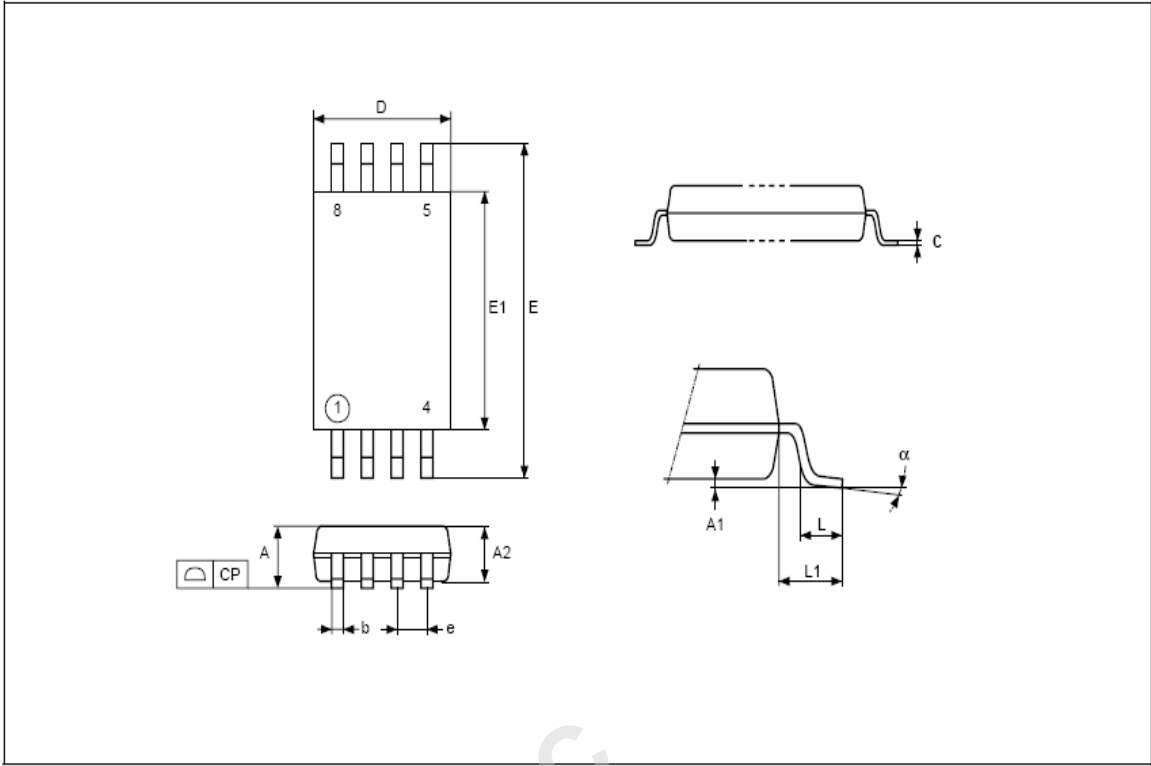
## TSSOP-8:  8-lead Thin Shrink Small Outline Package Outline



**Figure 17 — TSSOP-8 Package Outline**

**Table 27 — TSSOP-8 Package Dimensions**

| Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|
| A | -- | -- | 1.20 | mm |
| A1 | 0.50 | -- | 0.15 | mm |
| A2 | 0.80 | 1.00 | 1.05 | mm |
| b | 0.19 | -- | 0.30 | mm |
| c | 0.09 | -- | 0.20 | mm |
| CP | -- | -- | 1.00 | mm |
| D | 2.90 | 3.00 | 3.10 | mm |
| e | -- | 0.65 | -- | mm |
| E | 6.20 | 6.40 | 6.60 | mm |
| E1 | 4.30 | 4.40 | 4.50 | mm |
| L | 0.45 | 0.60 | 0.75 | mm |
| L1 | -- | 1.00 | -- | mm |
| $\alpha$ | 0 | -- | 8 | degrees |
| N | | 8 | | Leads |

Device Pinout

| | | | |
|---|---|---|---|
| SA0 | 1 | 8 | $V_{DDSPD}$ |
| SA1 | 2 | 7 | EVENT# |
| SA2 | 3 | 6 | SCL |
| $V_{SSSPD}$ | 4 | 5 | SDA |

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## 3. PACKAGING OPTIONS (cont'd)

### SOIC-8: 8-lead Ultra Thin Fine Pitch Dual Flat Package No Lead 5x6 mm Package Outline
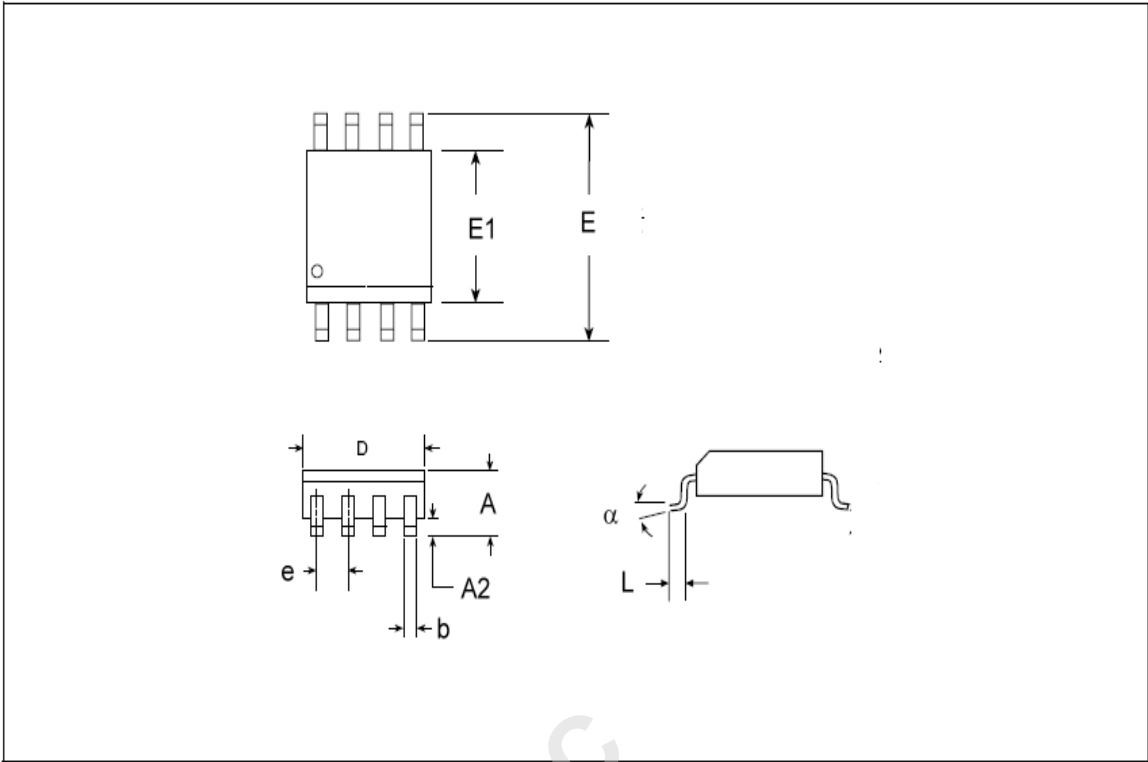


**Figure 18 — SOIC-8 Package Outline**

**Table 28 — SOIC-8 Package Dimensions**

| Symbol | Min | Typ | Max | Units |
|--------|-----|-----|-----|-------|
| A | 1.35 | 1.55 | 1.75 | mm |
| A2 | 0.10 | -- | 0.25 | mm |
| D | 4.80 | -- | 5.00 | mm |
| E | 5.80 | 6.00 | 6.20 | mm |
| E1 | 3.80 | -- | 4.00 | mm |
| b | 0.33 | -- | 0.51 | mm |
| e | -- | 1.27 | -- | mm |
| L | 0.40 | 0.45 | 0.50 | mm |
| $\alpha$ | 0 | -- | 8 | degrees |
| N | | 8 | | Leads |

Device Pinout

| | | | |
|--|--|--|--|
| SA0 | 1 | 8 | $V_{DDSPD}$ |
| SA1 | 2 | 7 | EVENT# |
| SA2 | 3 | 6 | SCL |
| $V_{SSSPD}$ | 4 | 5 | SDA |

## 3. PACKAGING OPTIONS (cont'd)

## MSOP-8:  8-lead Micro Small Outline 3x3 mm Package Outline
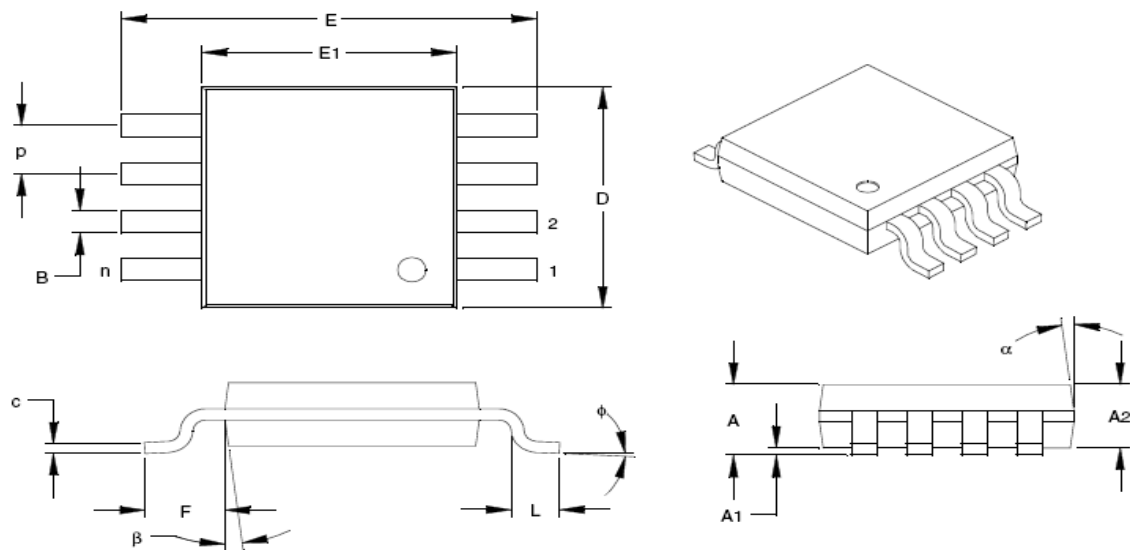


**Figure 19 — MSOP-8 Package Outline**

**Table 29 — MSOP-8 Package Dimensions**

| Symbol | Min | Typ | Max | Units |
|--------|-----|-----|-----|-------|
| A | -- | -- | 1.10 | mm |
| A1 | 0 | -- | 0.15 | mm |
| E | -- | 4.90 | -- | mm |
| E1 | -- | 3.00 | -- | mm |
| D | -- | 3.00 | -- | mm |
| L | 0.40 | 0.60 | 0.80 | mm |
| F | -- | 0.95 | -- | mm |
| c | 0.08 | -- | 0.23 | mm |
| p | -- | .65 | -- | mm |
| B | 0.22 | -- | 0.40 | mm |
| $\Phi$ | 0 | -- | 8 | degrees |
| $\alpha$ | 0 | -- | 8 | degrees |
| $\beta$ | 5 | -- | 15 | degrees |
| n | | 8 | | Leads |

Device Pinout

| | | | |
|-----|---|---|-----|
| SA0 | 1 | 8 | $V_{DDSPD}$ |
| SA1 | 2 | 7 | EVENT# |
| SA2 | 3 | 6 | SCL |
| $V_{SSSPD}$ | 4 | 5 | SDA |

## 3. PACKAGING OPTIONS (cont'd)

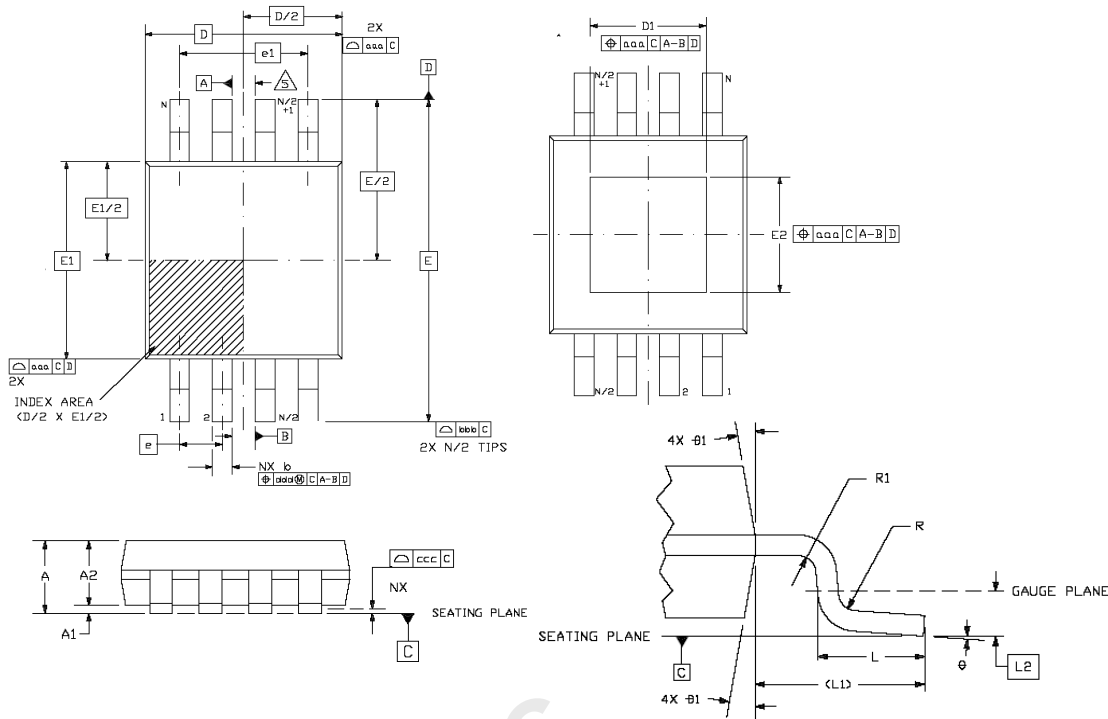### TSSOP-8 8-lead TSSOP 3x3 mm Package With Thermal Enhancement (MO-187)



**Figure 20 — TSSOP-8 Package Outline with Thermal Enhancement**

**Table 30 — TSSSOP-8 Package Dimensions**

| Symbol | Min | Typ | Max | Units |
|--------|-----|-----|-----|-------|
| A | -- | -- | 1.10 | mm |
| A1 | 0.0 | -- | 0.15 | mm |
| A2 | 0.75 | 0.85 | 0.95 | mm |
| D | 3.00 BSC | | | mm |
| D1 | 0.75 | -- | 2.50 | mm |
| E | 4.90 BSC | | | mm |
| E1 | 3.00 BSC | | | mm |
| E2 | 0.75 | -- | 2.50 | mm |
| e | 0.65 BSC | | | mm |
| e1 | 1.95 BSC | | | mm |
| L | 0.40 | 0.60 | 0.80 | mm |
| L1 | 0.95 REF | | | mm |
| R | 0.07 | -- | -- | mm |
| R1 | 0.07 | -- | -- | mm |
| $\theta$ | 0 | -- | 8 | degree |
| $\theta1$ | 5 | -- | 15 | degree |
| n | 8 | | | Leads |

Device Pinout

| | | | |
|---|---|---|---|
| SA0 | 1 | 8 | $V_{DDSPD}$ |
| SA1 | 2 | 7 | EVENT# |
| SA2 | 3 | 6 | SCL |
| $V_{SSSPD}$ | 4 | 5 | SDA |

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