4.1.2.9 – Appendix I: Specific SPD's for Virtual Channel SDRAM (VCSDRAM).

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1.0 Introduction: This appendix describes the Presence Detects for Virtual Channel Synchronous DRAM Modules with SPD revision level 2 (02h). These PD's are those referenced in the SPD standard document for "Specific Features". The following PD fields will occur, in the order presented, in table 1.1. Further descriptions of bytes 0 and 1 are found in the SPD standard. Further description of byte 2 is found in appendix A of the SPD standard.

1.1 Address map: The following is the SPD address map for VCSDRAM, which describes where the individual LUT–Entries/bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfgr	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	3
4	# Column Addresses on this assembly	9
5	# Module Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	VCSDRAM Cycle time at Max. Supported CAS Latency (CL), CL=X	4
10	VCSDRAM Access from Clock at CL=X	4
11	DIMM Configuration type (Non–parity, Parity, ECC)	
12	Refresh Rate/Type	4,5
13	VCSDRAM width, Primary DRAM	
14	Error Checking VCSDRAM data width	
15	Minimum Clock Delay, Back to Back Random Column Addresses	
16	Burst Lengths Supported	
17	# Banks on Each VCSDRAM device	4
18	CAS# Latencies Supported	4
19	CS# Latency	4
20	Write Latency	4
21	VCSDRAM Module Attributes	
22	VCSDRAM Device Attributes: General	
23	Minimum Clock Cycle Time at CL X–1	4
24	Maximum Data Access Time from Clock @ CL X–1	4
25	Minimum Clock Cycle Time at CL X–2	4
26	Maximum Data Access Time from Clock @ CL X–2	4
27	Minimum Row Precharge Time	4
28	Minimum Row Active to Row Active delay	4
29	Minimum Row Active to Prefetch Delay	4, 10
30	Minimum RAS Pulse Width	4
31	Module Bank Density	
32	Address and Command Setup time before Clock	6
33	Address and Command Hold time after Clock	6
34	Data Input Setup Time before Clock	6
35	Data Input Hold Time after Clock	6
36	Prefetch Read Latency	11
37	Minimum Prefetch to Read/Write Delay	11
38	Number of Segment Address	11
39	Number of Channel	11
40	Depth of Channels	11
41–61	Superset Information (may be used in future)	
62	SPD Revision	12
63	Checksum for bytes 0–62	
64–71	Manufacturers JEDEC ID code per JEP–106E	7
72	Manufacturing location	7
73–90	Manufacturer's Part Number	7
91–92	Revision Code	7
93–94	Manufacturing date	7
95–98	Assembly Serial Number	7
99–125	Manufacturer Specific Data	7
126–127	Vendor Specific	7
128–255	Open for Customer use.	8

notes:

1) This will be programmed as 128 bytes for the 168 pin DIMM Module.
2) This must be programmed as 256 bytes, 256 byte EEPROM's will be used for SPD on 168 pin VCSDRAM DIMMs.
3) High order bit defines if assembly has "redundant" addressing (if set to "1", highest order RAS# address must be re–sent as highest order CAS# address.)
4) From data sheet.
5) High order bit (MSB) is Self Refresh 'flag'. If bit seven is "1", assembly supports self refresh.
6) The JEDEC spec. specifies that these bytes are optional for 66MHz applications. If they are not included then the SPD revision level (byte 62) is set at revision 1 (01h).
7) The JEDEC spec specifies that these bytes are optional.
8) Module suppliers will need to assure that these bytes are open for reads/writes by Customer.
9) Including channel addresses. Usage of Column Addresses of VCSDRAM is different from SDRAM.
10) Changed from Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay in SDRAM.
11) Newly added for VCSDRAM. From Data Sheet
12) Revision level 2 (02h); This SPD contents for VCSDRAM are the same level of level 2 SPD for SDRAM

2.0 For Reference, Bytes 0 – 2. Descriptions of bytes 0 and 1 can be found in the main body of the SPD standard, and byte 2 is detailed in appendix A to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 BYTE 0, From General SPD Standard, Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 Byte 1, From General SPD Standard, Total SPD Memory Size: This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Invalid	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16384 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

2.3 Byte 2, From Appendix A, Memory Type: This byte describes the fundamental memory type (or technology) implemented on the module:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
.	.	.	.	.	.	.	.	.
VCSDRAM	0	0	0	0	1	0	0	0

3.0 Data Type(s): Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.

4.0 The following PD bytes are those specific to modules implementing Synchronous DRAM technology. Note that these full descriptions start at byte 3 below and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology

4.1 Byte 3, Number of ROW Addresses: This field describes the Row addressing on the module. If there is one physical bank on the module OR if there are two physical banks of the same size and organization, then bits 0–3 are used to represent the number of row addresses for each physical bank. If the module has two physical banks of asymmetric size, then bits 0–3 represent the number of row addresses for physical bank 1 and bits 4–7 represent the number of row addresses for physical bank 2. Note that these do not include the Bank Address pin since physical bank selection on DIMM modules is asserted on dedicated BA (Bank Address) pins. Also note that if the module employs redundant addressing, then it is denoted in Byte 21, bit 6. Examples of Byte 3 implementation include:

#Banks	# Row Addr Bank 1	# Row Addr Bank2	Module Orgainzation	Discrete Used	Byte 3 Contents
1	11,RA0–RA10	N/A	2Mx64	2Mx8	0000 1011
2	11,RA0–RA10	11,RA0–RA10	2x2Mx64	2Mx8	0000 1011
2	11,RA0–RA10	11,RA0–RA10	2Mx64 & 1Mx64	2Mx8 & 1Mx16	1011 1011

# Row Addr					Table Subfield A: No. of Row addresses on Bank 1 –OR– No. of Row addresses on Bank 1 and 2 if both banks have the same depth, bits 0–3			
					Bit 3	Bit 2	Bit 1	Bit 0
Undefined	See Subfield B				0	0	0	0
1/16					0	0	0	1
2/17					0	0	1	0
:					:	:	:	:
7					0	1	1	1
8					1	0	0	0
9					1	0	0	1
10					1	0	1	0
11					1	0	1	1
12					1	1	0	0
13					1	1	0	1
14					1	1	1	0
15					1	1	1	1
# Row Addr	Table Subfield B: Number of Row addresess on Bank 2 (if different from bank 1), bits 4–7				See Subfield A			
	Bit 7	Bit 6	Bit5	Bit 4				
No 2nd Asymmetrical bank	0	0	0	0				
1/16	0	0	0	1				
2/17	0	0	1	0				
:	:	:	:	:				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				
11	1	0	1	1				
12	1	1	0	0				
13	1	1	0	1				
14	1	1	1	0				
15	1	1	1	1				

4.2 Byte 4, Number of Column Addresses: This field describes the Column addressing on the module. Even though usage of Column address of VCSDRAM is different from SDRAM, in order to keep consistency, the number of addresses used in READ or WRITE command should be written. (ie. Including channel addresses.) If there is one physical bank on the module OR if there are two physical banks of the same size, then bits 0–3 are used to represent the number of column addresses for each physical bank. If the module has two physical banks of asymmetric size, then bits 0–3 represent the number of column addresses for physical bank 1 and bits 4–7 represent the number of column addresses for physical bank 2.

#Banks	# Col Addr Bank 1	# Col AddrModule Bank2	Discrete Organization	Used	Byte 3 Contents
1	9,CA0–CA8	N/A	2Mx64	2Mx8	0000 1001
2	9,CA0–CA8	9,CA0–CA8	2x2Mx64	2Mx8	0000 1001
2	9,CA0–CA8	8,CA0–CA7	2Mx64 & 1Mx64	2Mx8 & 1Mx16	1000 1001

# Column Addr		Table Subfield A: No. of Column addresses on Bank 1 –OR– No. of Column addresses on Bank 1 and 2 if both banks same depth, bits 0–3			
		Bit 3	Bit 2	Bit 1	Bit 0
Undefined	See Subfield B	0	0	0	0
1/16		0	0	0	1
2/17		0	0	1	0
:		:	:	:	:
7		0	1	1	1
8		1	0	0	0
9		1	0	0	1
10		1	0	1	0
11		1	0	1	1
12		1	1	0	0
13		1	1	0	1
14		1	1	1	0
15		1	1	1	1

# Column Addr	Table Subfield B: Number of Column addresess on Bank 2 (if different from bank 1), bits 4–7				
	Bit 7	Bit 6	Bit5	Bit 4	
No 2nd Asymmetrical bank	0	0	0	0	See Subfield A
1/16	0	0	0	1	
2/17	0	0	1	0	
:	:	:	:	:	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

4.3 Byte 5, Number of Banks on module: This field describes the number of physical banks on the VCSDRAM Module. This is not to be confused with the number of logical banks on a given VCSDRAM device which are defined in Byte 17:

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4 Bytes 6 & 7, Module Data Width: Bytes 6 and 7 are used to designate the module's data width. The data width is presented as a 16 bit word; bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit 7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits wide, byte 7 will be 00h. If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width. For example, if the module's

data width is:	then byte 7 is	and byte 6 is:
64	0000 0000	0100 0000
72	0000 0000	0100 1000
80	0000 0000	0101 0000
576	0000 0010	0100 0000

4.4.1 Byte 6:

Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
80	0	1	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4.2 Byte 7, Module Data Width Continued: This byte will be left at 00h if the original module data width is less than 256 bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6.

Module Data Width Cont.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	X
1024(+)	0	0	0	0	0	1	X	X
2048(+)	0	0	0	0	1	X	X	X
.	.	.	.	.	.	.	.	.

4.5 Byte 8, Module Interface Levels: This field describes the module’s voltage interface:

Voltage Interface	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5 V	0	0	0	0	0	0	1	0
SSTL 3.3 V	0	0	0	0	0	0	1	1
SSTL 2.5 V	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	1	1	1	1	1	1	1	1

4.6 Byte 9, VCSDRAM Cycle time (tCYC): This byte defines the minimum cycle time for the VCSDRAM Module at the highest $\overline{\text{CAS}}$ Latency, $\overline{\text{CAS}}$ Latency=X, defined in byte 18. If other $\overline{\text{CAS}}$ latencies are supported, then the associated minimum cycle times are written into byte 23 and 25. Byte 9, Cycle time for $\overline{\text{CAS}}$ Latency = X, is split into two nibbles: the higher order nibble (bits 4 through 7) designate the cycle time to a granularity of 1 ns; the value presented by the lower order nibble (bits 0 through 3) has a granularity of 1/10 ns and is added to the value designated by the higher nibble. For example, if

Bits 7:4 are	and bits 3:0 are	then the cycle time is
1010	0101	(10 ns) + (0.5 ns) = 10.5 ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCSDRAM Cycle Time Subfield A: Units of nanoseconds (bits 4 through 7)								
Undefined	0	0	0	0				
1 ns	0	0	0	1				
2 ns	0	0	1	0				
3 ns	0	0	1	1				
4 ns	0	1	0	0				
5 ns	0	1	0	1	SEE Subfield Table B			
6 ns	0	1	1	0				
7 ns	0	1	1	1				
8 ns	1	0	0	0				
9 ns	1	0	0	1				
10 ns	1	0	1	0				
11 ns	1	0	1	1				
12 ns	1	1	0	0				
13 ns	1	1	0	1				
14 ns	1	1	1	0				
15 ns	1	1	1	1				
VCSDRAM Cycle Time Subfield B: Tenths of ns (bits 0 through 3)								
+0 ns					0	0	0	0
+0.1 ns					0	0	0	1
+0.2 ns					0	0	1	0
+0.3 ns					0	0	1	1
+0.4 ns					0	1	0	0
+0.5 ns	SEE Subfield table A				0	1	0	1
+0.6 ns					0	1	1	0
+0.7 ns					0	1	1	1
+0.8 ns					1	0	0	0
+0.9 ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
Undefined	1	1	1	1	1	1	1	1

4.7 Byte 10, VCSDRAM Access time from Clock (tAC): This byte defines the maximum clock to data out for the module. This is the Clock to data out specification at the highest given $\overline{CAS}$ Latency specified/depicted in byte 18 of this SPD specification/standard. If other $\overline{CAS}$ latencies are supported, then the associated Maximum Clock Access times are written into bytes 24 and 26.

The byte is split into two nibbles: the higher order nibble (bits 4 through 7) designate the cycle time to a granularity of 1 ns; the value presented by the lower order nibble (bits 0 through 3) has a granularity of 1/10 ns and is added to the value designated by the higher nibble. For example, if

Bits 7:4 are	and bits 3:0 are	then the cycle time is
1001	0000	(9 ns) + (0.0 ns) = 9.0 ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	VCSDRAM Access time from Clock: Subfield A: Units of nanoseconds (bits 4 through 7)							
Undefined	0	0	0	0	SEE Subfield Table B			
1 ns	0	0	0	1				
2 ns	0	0	1	0				
3 ns	0	0	1	1				
4 ns	0	1	0	0				
5 ns	0	1	0	1				
6 ns	0	1	1	0				
7 ns	0	1	1	1				
8 ns	1	0	0	0				
9 ns	1	0	0	1				
10 ns	1	0	1	0				
11 ns	1	0	1	1				
12 ns	1	1	0	0				
13 ns	1	1	0	1				
14 ns	1	1	1	0				
15 ns	1	1	1	1				
	VCSDRAM Access time from CLK Subfield B: Tenths of ns (bits 0 through 3)							
+0ns	SEE Subfield table A				0	0	0	0
+0.1 ns					0	0	0	1
+0.2 ns					0	0	1	0
+0.3 ns					0	0	1	1
+0.4 ns					0	1	0	0
+0.5 ns					0	1	0	1
+0.6 ns					0	1	1	0
+0.7 ns					0	1	1	1
+0.8 ns					1	0	0	0
+0.9 ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
Undefined	1	1	1	1	1	1	1	1

4.8 Byte 11, Module Configuration type: This field describes the module's error detection and or correction schemes:

Error Det/Cor	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	1

4.9 Byte 12, Refresh Rate/Type: This field describes the module's refresh rate and type:

Refresh Period	Bit 7, Self Refresh Flag	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal (15.625 us)	0	0	0	0	0	0	0	0
Reduced (.25x)...3.9 us	0	0	0	0	0	0	0	1
Reduced (.5x)...7.8 us	0	0	0	0	0	0	1	0
Extended (2x)...31.3 us	0	0	0	0	0	0	1	1
Extended (4x)...62.5 us	0	0	0	0	0	1	0	0
Extended (8x)...125 us	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
TBD	0	0	0	0	0	1	1	1
TBD	0	0	0	0	1	0	0	0
TBD	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
Self Refresh Entries								
Normal (15.625 us)	1	0	0	0	0	0	0	0
Reduced (0.25x)...3.9 us	1	0	0	0	0	0	0	1
Reduced (0.5x)...7.8 us	1	0	0	0	0	0	1	0
Extended (2x)...31.3 us	1	0	0	0	0	0	1	1
Extended (4x)...62.5 us	1	0	0	0	0	1	0	0
Extended (8x)...125 us	1	0	0	0	0	1	0	1
TBD	1	0	0	0	0	1	1	0
TBD	.	.	.	.	.	.	.	.
TBD	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	0
TBD	1	1	1	1	1	1	1	1

4.10 Byte 13, VCSDRAM width, Primary VCSDRAM: Bits 0–6 of this byte relate the primary data VCSDRAM's width; bit 7 is a flag which is set to "1" when there is a 2nd physical bank on the module which is of different size from the 1st physical bank. Bit 7 set to "1" indicates that the 2nd physical bank's data RAMs are 2X the width of those on the 1st physical bank. If there is a second physical bank of same size and organization as the first , then bit 7 remains as "0" and error checking VCSDRAM width for both banks is expressed using bits 0–6. The primary VCSDRAM is that which is used for data; examples of primary (data) VCSDRAM widths are x4, x8, x16, x32. Note that if the module is made with VCSDRAMs which provide for data and error checking e.g. x9, x18, x36, then it is also designated in this field. Examples of VCSDRAM DIMM using 1 and 2 banks of symmetrical and asymmetrical size:

Module Width	Physical Bank 1 Primary VCSDRAM Width	Physical Bank 2 Primary VCSDRAM Width	Physical Bank 1 Error Checking VCSDRAM Width	Physical Bank 2 Error Checking VCSDRAM Width	Possible (16Mb based) Module Density	Byte 13 Contents
x72	x9	N/A	—	N/A	16 MB	0000 1001
x72	x8	N/A	x8	N/A	16 MB	0000 1000
x72	x16	N/A	x4	N/A	8 MB	0001 0000
x72	x8	x8	x8	x8	32 MB	0000 1000
x64	x8	x16	N/A	N/A	24 MB	1000 1000

Subfield A: Data VCSDRAM Width								
Data VCSDRAM Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	See Subfield B	0	0	0	0	0	0	0
1		0	0	0	0	0	0	1
:		:	:	:	:	:	:	:
4		0	0	0	0	1	0	0
:		:	:	:	:	:	:	:
8		0	0	0	1	0	0	0
9		0	0	0	1	0	0	1
:		:	:	:	:	:	:	:
15		0	0	0	1	1	1	1
16		0	0	1	0	0	0	0
17		0	0	1	0	0	0	1
:		:	:	:	:	:	:	:
32		0	1	0	0	0	0	0
:		:	:	:	:	:	:	:
36		0	1	0	0	1	0	0
:		:	:	:	:	:	:	:
127		1	1	1	1	1	1	1
Subfield B: Bank 2 Data VCSDRAM Width Multiplier								
Bank 2 Data VCSDRAM Width Multiplier	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
No Bank 2 –OR– Bank 2 uses same width VCSDRAM as bank 1	0	See Subfield A						
Bank 2 VCSDRAM is 2X the Width of Bank 1 VCSDRAM	1							

4.11 Byte 14, Error Checking VCSDRAM data width: If the module incorporates error checking and if the primary data VCSDRAM does not include these bits; i.e. there are separate error checking VCSDRAMs, then the error checking VCSDRAM's width is expressed in this byte. Bits 0–6 of this byte relate the error checking VCSDRAMs width; bit 7 is a flag which is set to "1" when there is a 2nd physical bank on the module which is of different size from the 1st physical bank. Bit 7 set to "1" indicates that Bank 2's error checking RAMs are 2X the width of those on the 1st physical bank. If there is a second physical bank of same size and organization as the first , then bit 7 remains as "0" and error checking VCSDRAM width for both physical banks is expressed using bits 0–6. Examples of error checking VCSDRAM widths with 1 and 2 physical banks of Symmetric and Asymmetric sizing include:

Module Width	Physical Bank 1 Primary VCSDRAM Width	Physical Bank 2 Primary VCSDRAM Width	Physical Bank 1 Error Checking VCSDRAM Width	Physical Bank 2 Error Checking VCSDRAM Width	Possible (16Mb based) Module Density	Byte 14 Contents
x72	x9	N/A	—	N/A	16 MB	0000 0000
x72	x8	N/A	x8	N/A	16 MB	0000 1000
x72	x16	N/A	x4	N/A	8 MB	0000 0100
x72	x8	x8	x8	x8	32 MB	0000 1000
x72	x8	x16	x8	x16	24 MB	1000 1000
x80	x8	x16	x8	x16	24 MB	1000 1000

Subfield A: Error Checking VCSDRAM Width								
Error Checking VCSDRAM Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	See Subfield B	0	0	0	0	0	0	0
1		0	0	0	0	0	0	1
:		:	:	:	:	:	:	:
4		0	0	0	0	1	0	0
:		:	:	:	:	:	:	:
8		0	0	0	1	0	0	0
9		0	0	0	1	0	0	1
:		:	:	:	:	:	:	:
15		0	0	0	1	1	1	1
16		0	0	1	0	0	0	0
17		0	0	1	0	0	0	1
:		:	:	:	:	:	:	:
32		0	1	0	0	0	0	0
:		:	:	:	:	:	:	:
36		0	1	0	0	1	0	0
:		:	:	:	:	:	:	:
63		1	1	1	1	1	1	1

Subfield B: Bank 2 Error Checking VCSDRAM Width Multiplier								
Bank 2 Error Checking VCSDRAM Width Multiplier	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
No Bank 2 –OR– Bank 2 uses same width VCSDRAM as bank 1	0	See Subfield A						
Bank 2 VCSDRAM is 2X the Width of Bank 1 VCSDRAM	1							

4.12 Byte 15, VCSDRAM Device Attributes: Minimum Clock Delay, Back to Back Random Column Accesses. Note that VCSDRAM architecture can be gained with this parameter.

Number of Clocks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
.	.					.		
255	1	1	1	1	1	1	1	1

4.13 Byte 16, VCSDRAM Device Attributes, Burst Lengths Supported: This byte describes which various programmable burst lengths are supported by the devices on the module. If the bit is “1”, then that Burst Length is supported on the module; If the bit is “0”, then that burst length is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Burst Length = Page	TBD	TBD	Burst Length = 16	Burst Length = 8	Burst Length = 4	Burst Length = 2	Burst Length = 1
1 or 0	0	0	0	1 or 0	1 or 0	1 or 0	1 or 0

4.14 Byte 17, VCSDRAM Device Attributes, Number of Banks on the discrete VCSDRAM Device: This byte details how many banks are on each discrete VCSDRAM installed onto the module:

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
.	.					.		
255	1	1	1	1	1	1	1	1

4.15 Byte 18, VCSDRAM Device Attributes, CAS# Latency: This byte describes which of the programmable CAS# Latencies are supported by the Module. If the bit is “1”, then that CAS# Latency is supported on the module; If the bit is “0”, then that CAS# Latency is not supported by the module. Bytes 9,10,23–26 all relate CAS Latency dependent timings.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	CAS# Latency = 7	CAS# Latency = 6	CAS# Latency = 5	CAS# Latency = 4	CAS# Latency = 3	CAS# Latency = 2	CAS# Latency = 1
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.16 Byte 19, VCSDRAM Device Attributes, CS# Latency: This byte describes which of the programmable CS# Latencies are acceptable for the Module. If the bit is “1”, then that CS# Latency is supported on the module; If the bit is “0”, then that CS# Latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	CS# Latency = 6	CS# Latency = 5	CS# Latency = 4	CS# Latency = 3	CS# Latency = 2	CS# Latency = 1	CS# Latency = 0
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.17 Byte 20, VCSDRAM Device Attributes, WE# Latency: This byte describes which of the programmable WE# Latencies are acceptable for the Module. If the bit is “1”, then that WE# Latency is supported on the module; If the bit is “0”, then that WE# Latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	WE# Latency = 6	WE# Latency = 5	WE# Latency = 4	WE# Latency = 3	WE# Latency = 2	WE# Latency = 1	WE# Latency = 0
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

4.18 Byte 21, VCSDRAM Module Attributes: This byte depicts various aspects of the module. It details various unrelated but critical elements pertinent to the module. A given module characteristic is detailed in the designated bit; if the aspect is TRUE, then the bit is “1”. Conversely, if the aspect is FALSE, then the designated bit is “0”.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	*Redundant Addressing	Differential Clock Input	Registered DQMB Inputs	Buffered DQMB Inputs	On–Card PLL (Clock)	**Registered Address and Control Inputs	**Buffered Address and Control Inputs
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

* Redundant addressing implies the use of VCSDRAMs having the same address depth (e.g. 4Mx4 mixed with 4Mx16) in the same 8 byte quad word, but having different RAS/CAS addressing and/or different numbers of device banks. Actual implementation is not yet determined.

** Address, RAS, CAS, WE, CKE, CS

4.19 Byte 22, VCSDRAM Device Attributes, General: This byte depicts various aspects of the VCSDRAMs on the module. It details various unrelated but critical elements pertinent to the VCSDRAMs. A given VCSDRAM characteristic is detailed in the designated bit; unless otherwise specified, if the aspect is TRUE, then the bit is “1”. Conversely, if the aspect is FALSE, then the designated bit is “0”.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	*Upper Vcc tolerance: 0=10% 1=5%	*Lower Vcc tolerance: 0=10% 1=5%	Supports Write1/Read Burst 0=false 1=true	Supports Precharge All 0=false 1=true	Supports Auto–Precharge 0=false 1=true	Supports Early RAS# Precharge 0=false 1=true
0	0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

* Tolerance refers to the voltage range under which the VCSDRAMs operate.

** Early $\overline{RAS}$ Precharge is supported by all devices. This bit can only be a “1”.

4.20 Byte 23: Minimum Clock Cycle Time at reduced CAS latency, X–1: The highest CAS latency identified in byte 18 is X and the timing values associated with CAS Latency 'X' are found at byte locations 9 and 10. Byte 23 denotes the minimum cycle time at CAS X–1.

For example, if byte 18 denotes CAS latencies of 1–3, then X is 3 and X–1 is 2. Byte 23 then denotes the minimum cycle time at CAS Latency = 2.

Byte 23 is split into two nibbles: the higher order nibble (bits 4 through 7) designate the cycle time to a granularity of 1 ns; the value presented by the lower order nibble (bits 0 through 3) has a granularity of 1/10 ns and is added to the value designated by the higher nibble. For example, if

Bits 7:4 are	and bits 3:0 are	then the cycle time is
1001	0101	(9 ns) + (0.5 ns) = 9.5 ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCSDRAM Minimum Cycle time @ CL X–1: Subfield A: In units of ns (bits 4 through 7)								
Undefined	0	0	0	0	SEE Subfield Table B			
1 ns/16 ns	0	0	0	1				
2 ns/17 ns	0	0	1	0				
3 ns/18 ns	0	0	1	1				
4 ns	0	1	0	0				
5 ns	0	1	0	1				
6 ns	0	1	1	0				
7 ns	0	1	1	1				
8 ns	1	0	0	0				
9 ns	1	0	0	1				
10 ns	1	0	1	0				
11 ns	1	0	1	1				
12 ns	1	1	0	0				
13 ns	1	1	0	1				
14 ns	1	1	1	0				
15 ns	1	1	1	1				
VCSDRAM Minimum Cycle time @ CL X–1: Subfield B: Tenths of ns (bits 0 through 3)								
+0 ns	SEE Subfield table A				0	0	0	0
+0.1 ns					0	0	0	1
+0.2 ns					0	0	1	0
+0.3 ns					0	0	1	1
+0.4 ns					0	1	0	0
+0.5 ns					0	1	0	1
+0.6 ns					0	1	1	0
+0.7 ns					0	1	1	1
+0.8 ns					1	0	0	0
+0.9 ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
Undefined	1	1	1	1	1	1	1	1

4.21 Byte 24: Maximum Data Access Time from Clock (tAC) at Reduced CAS Latency, X–1: The highest CAS latency identified in byte 18 is X.. Byte 24 denotes the maximum access time from Clock at CAS Latency X–1.

For example, if byte 18 denotes supported CAS latencies of 1–3, then X is 3 and
X–1 is 2. Byte 24 then denotes the maximum data access time from CLK at CAS Latency 2.

The byte is split into two nibbles: the higher order nibble (bits 4 through 7) designate the cycle time to a granularity of 1 ns; the value presented by the lower order nibble (bits 0 through 3) has a granularity of 1/10 ns and is added to the value designated by the higher nibble. For example, if

Bits 7:4 are	and bits 3:0 are	then the cycle time is
1001	0101	(9 ns) + (0.5 ns) = 9.5 ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCSDRAM Access time from Clock @ CL X–1: Subfield A: Units of nanoseconds (bits 4 through 7)								
Undefined	0	0	0	0	SEE Subfield Table B			
1 ns/16 ns	0	0	0	1				
2 ns/17 ns	0	0	1	0				
3 ns/18 ns	0	0	1	1				
4 ns	0	1	0	0				
5 ns	0	1	0	1				
6 ns	0	1	1	0				
7 ns	0	1	1	1				
8 ns	1	0	0	0				
9 ns	1	0	0	1				
10 ns	1	0	1	0				
11 ns	1	0	1	1				
12 ns	1	1	0	0				
13 ns	1	1	0	1				
14 ns	1	1	1	0				
15 ns	1	1	1	1				
VCSDRAM Access time from CLK @ CL X–1 Subfield B: Tenths of ns (bits 0 through 3)								
+0 ns	SEE Subfield table A				0	0	0	0
+0.1 ns					0	0	0	1
+0.2 ns					0	0	1	0
+0.3 ns					0	0	1	1
+0.4 ns					0	1	0	0
+0.5 ns					0	1	0	1
+0.6 ns					0	1	1	0
+0.7 ns					0	1	1	1
+0.8 ns					1	0	0	0
+0.9 ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
Undefined	1	1	1	1	1	1	1	1

4.22 Byte 25: Minimum Clock Cycle time at reduced CAS latency, X–2: The highest CAS latency identified in byte 18 is X.. Byte 25 denotes the minimum cycle time at CAS Latency X–2.

For example, if byte 18 denotes CAS latencies of 1–3, then X is 3 and X–2 is 1. Byte 25 then denotes the minimum cycle time at CAS Latency 1.

Byte 25 is split into two parts: the higher order bits (bits 2 through 7) designate the cycle time to a granularity of 1 ns; the value presented by the lower order bits (0 through 1) has a granularity of 1/4 ns and is added to the value designated by the higher bits. For example, if

Bits 7:2 are	and bits 1:0 are	then the cycle time is
011001	00	(25 ns) + (0.0 ns) = 25.0 ns
Bits 7:2 are	and bits 1:0 are	then the cycle time is
100001	11	(33 ns) + (.75 ns) = 33.75 ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	VCSDRAM Minimum Cycle time @ CL X–2: Subfield A: In units of ns (bits 2 through 7)						See Subfield B	
Undefined	0	0	0	0	0	0		
1 ns	0	0	0	0	0	1		
2 ns	0	0	0	0	1	0		
3 ns	0	0	0	0	1	1		
4 ns	0	0	0	1	0	0		
5 ns	0	0	0	1	0	1		
6 ns	0	0	0	1	1	0		
7 ns	0	0	0	1	1	1		
8 ns	0	0	1	0	0	0		
9 ns	0	0	1	0	0	1		
10 ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61 ns	1	1	1	1	0	1		
62 ns	1	1	1	1	1	0		
63 ns	1	1	1	1	1	1		
							VCSDRAM Minimum Cycle time @ CL = X–2 Field B: Quarters of ns (bits 0 through 1)	
+0 ns	SEE Subfield table A						0	0
+0.25 ns							0	1
+0.5 ns							1	0
+0.75 ns							1	1

4.23 Byte 26: Maximum Data Access Time from Clock (tAC) at reduced CAS Latency, X–2: The highest CAS latency identified in byte 18 is X.. Byte 26 denotes the maximum access time from Clock at CAS Latency X–2.

For example, if byte 18 denotes supported CAS latencies of 1–3, then X is 3 and
X–2 is 1. Byte 26 then denotes the maximum data access time from CLK at CAS Latency 1.

The byte is split into two parts: the higher order bits (bits 2 through 7) designate the cycle time to a granularity of 1 ns; the value presented by the lower order nibble (bits 0 through 1) has a granularity of 1/4 ns and is added to the value designated by the higher nibble. For example, if

Bits 7:2 are	and bits 1:0 are	then the max access time is
001001	01	(9 ns) + (0.25 ns) = 9.25 ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	VCSDRAM Access time from Clock @ CL X–2: Subfield A: Units of nanoseconds (bits 4 through 7)						See Subfield B	
Undefined	0	0	0	0	0	0		
1 ns	0	0	0	0	0	1		
2 ns	0	0	0	0	1	0		
3 ns	0	0	0	0	1	1		
4 ns	0	0	0	1	0	0		
5 ns	0	0	0	1	0	1		
6 ns	0	0	0	1	1	0		
7 ns	0	0	0	1	1	1		
8 ns	0	0	1	0	0	0		
9 ns	0	0	1	0	0	1		
10 ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61 ns	1	1	1	1	0	1		
62 ns	1	1	1	1	1	0		
63 ns	1	1	1	1	1	1		
							VCSDRAM Access time from CLK @ CL X–2 Subfield B: Quarters of ns (bits 0 through 1)	
+0 ns	SEE Subfield table A						0	0
+0.25 ns							0	1
+0.5 ns							1	0
+0.75 ns							1	1

4.24 Byte 27, Minimum Row Precharge Time (tRP): Byte 27 is used to designate the modules minimum Row Precharge time. The decode for this SPD byte is as follows:

Minimum Row Precharge time (Nanoseconds)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
31	0	0	0	1	1	1	1	1
32	0	0	1	0	0	0	0	0
33	0	0	1	0	0	0	0	1
34	0	0	1	0	0	0	1	0
35	0	0	1	0	0	0	1	1
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.25 Byte 28, Minimum Row Active to Row Active Delay (tRRD): This field describes the minimum required delay between different row activations:

Min Row active to Row Active Delay (Nanoseconds)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
19	0	0	0	1	0	0	1	1
20	0	0	0	1	0	1	0	0
21	0	0	0	1	0	1	0	1
22	0	0	0	1	0	1	1	0
23	0	0	0	1	0	1	1	1
24	0	0	0	1	1	0	0	0
25	0	0	0	1	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.26 Byte 29, Minimum Row Active to Prefetch Delay (tAPD): This SPD byte describes the minimum delay required between assertions of Row Active and Prefetch command.

Minimum Row Active to Prefetch Delay (Nanoseconds)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
31	0	0	0	1	1	1	1	1
32	0	0	1	0	0	0	0	0
33	0	0	1	0	0	0	0	1
34	0	0	1	0	0	0	1	0
35	0	0	1	0	0	0	1	1
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.27 Byte 30: tRAS: This byte identifies the minimum delay required between row active and precharge command for the same bank.

Minimum RAS Pulse Width (Nanoseconds)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
31	0	0	0	1	1	1	1	1
32	0	0	1	0	0	0	0	0
33	0	0	1	0	0	0	0	1
34	0	0	1	0	0	0	1	0
35	0	0	1	0	0	0	1	1
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.28: Byte 31: Density of each bank on module: This byte describes the density of each physical bank on the VCSDRAM DIMM. This byte will have at least one bit set to “1” to represent at least one banks density. If there are more than one bank on the module (as represented in byte #5) and they have the same density, then only one bit is set in this field. If the module has more than one bank of different sizes then more than one bit will be set; each bit set for each density represented. For example:

# Banks	Densiy of Bank 1	Density of bank 2	Byte 31 contents
1	32 M Byte	N/A	0000 1000
2	32 M Byte	32 M Byte	0000 1000
2	32 M Byte	16 M Byte	0000 1100

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Density	512 M Byte	256 M Byte	128 M Byte	64 M Byte	32 M Byte	16 M Byte	8 M Byte	4 M Byte
N/Y	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

4.29 Byte 32, Address and Command signal input setup time before clock: This field describes the input setup time before the rising edge of clock. Since this value can be either negative or positive, provisions have been made to accomodate both. If one byte starts with a Zero in bit 7, then the input setup time is positive. If the byte starts with a One in bit 7, then the value is negative.
For example, if

Value	Byte Contents
2.5 ns	0010 0101
–2.5 ns	1010 0101

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Setup Time before Clock: Subfield A: Units of nanoseconds (bits 4 through 7)								
Less than 1 ns, >0	0	0	0	0	SEE Subfield Table B			
1 ns	0	0	0	1				
2 ns	0	0	1	0				
3 ns	0	0	1	1				
4 ns	0	1	0	0				
5 ns	0	1	0	1				
6 ns	0	1	1	0				
7 ns	0	1	1	1				
Less than zero, > (–1 ns)	1	0	0	0				
–1 ns	1	0	0	1				
–2 ns	1	0	1	0				
–3 ns	1	0	1	1				
–4 ns	1	1	0	0				
–5 ns	1	1	0	1				
–6 ns	1	1	1	0				
–7 ns	1	1	1	1				
Input Setup Time before Clock: Subfield B: Tenths of ns (bits 0 through 3)								
+/–0 ns	SEE Subfield table A				0	0	0	0
+/–0.1 ns					0	0	0	1
+/–0.2 ns					0	0	1	0
+/–0.3 ns					0	0	1	1
+/–0.4 ns					0	1	0	0
+/–0.5 ns					0	1	0	1
+/–0.6 ns					0	1	1	0
+/–0.7 ns					0	1	1	1
+/–0.8 ns					1	0	0	0
+/–0.9 ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
RFU	1	1	1	1	1	1	1	1

4.30 Byte 33, Address and Command signal input hold times after clock: This field describes the input hold time after the rising edge of clock. Since this value can be either negative or positive, provisions have been made to accomodate both. If one byte starts with a Zero in bit 7, then the input setup time is positive. If the byte starts with a One in bit 7, then the value is negative.

For example, if

Value	Byte Contents
2.5 ns	0010 0101
–2.5 ns	1010 0101

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Hold times after Clock: Subfield A: Units of nanoseconds (bits 4 through 7)								
Less than 1 ns, >0	0	0	0	0	SEE Subfield Table B			
1 ns	0	0	0	1				
2 ns	0	0	1	0				
3 ns	0	0	1	1				
4 ns	0	1	0	0				
5 ns	0	1	0	1				
6 ns	0	1	1	0				
7 ns	0	1	1	1				
Less than zero, > (–1 ns)	1	0	0	0				
–1 ns	1	0	0	1				
–2 ns	1	0	1	0				
–3 ns	1	0	1	1				
–4 ns	1	1	0	0				
–5 ns	1	1	0	1				
–6 ns	1	1	1	0				
–7 ns	1	1	1	1				
Input Hold times after Clock: Subfield B: Tenths of ns (bits 0 through 3)								
+/–0 ns	SEE Subfield table A				0	0	0	0
+/–0.1 ns					0	0	0	1
+/–0.2 ns					0	0	1	0
+/–0.3 ns					0	0	1	1
+/–0.4 ns					0	1	0	0
+/–0.5 ns					0	1	0	1
+/–0.6 ns					0	1	1	0
+/–0.7 ns					0	1	1	1
+/–0.8 ns					1	0	0	0
+/–0.9 ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
RFU	1	1	1	1	1	1	1	1

4.31 Byte 34, Data Signal input setup time before clock: This field describes the input setup time before the rising edge of clock. Since this value can be either negative or positive, provisions have been made to accomodate both. If one byte starts with a Zero in bit 7, then the input setup time is positive. If the byte starts with a One in bit 7, then the value is negative.
For example, if

Value	Byte Contents
2.5 ns	0010 0101
–2.5 ns	1010 0101

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Setup Time before Clock: Subfield A: Units of nanoseconds (bits 4 through 7)								
Less than 1 ns, >0	0	0	0	0	SEE Subfield Table B			
1 ns	0	0	0	1				
2 ns	0	0	1	0				
3 ns	0	0	1	1				
4 ns	0	1	0	0				
5 ns	0	1	0	1				
6 ns	0	1	1	0				
7 ns	0	1	1	1				
Less than zero, > (–1 ns)	1	0	0	0				
–1 ns	1	0	0	1				
–2 ns	1	0	1	0				
–3 ns	1	0	1	1				
–4 ns	1	1	0	0				
–5 ns	1	1	0	1				
–6 ns	1	1	1	0				
–7 ns	1	1	1	1				
Input Setup Time before Clock: Subfield B: Tenths of ns (bits 0 through 3)								
+/–0 ns	SEE Subfield table A				0	0	0	0
+/–0.1 ns					0	0	0	1
+/–0.2 ns					0	0	1	0
+/–0.3 ns					0	0	1	1
+/–0.4 ns					0	1	0	0
+/–0.5 ns					0	1	0	1
+/–0.6 ns					0	1	1	0
+/–0.7 ns					0	1	1	1
+/–0.8 ns					1	0	0	0
+/–0.9 ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
RFU	1	1	1	1	1	1	1	1

4.32 Byte 35, Data Signal Input hold times after clock: This field describes the input hold time after the rising edge of clock. Since this value can be either negative or positive, provisions have been made to accomodate both. If one byte starts with a Zero in bit 7, then the input setup time is positive. If the byte starts with a One in bit 7, then the value is negative.
For example, if

Value	Byte Contents
2.5 ns	0010 0101
–2.5 ns	1010 0101

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Hold times after Clock: Subfield A: Units of nanoseconds (bits 4 through 7)								
Less than 1 ns, >0	0	0	0	0	SEE Subfield Table B			
1 ns	0	0	0	1				
2 ns	0	0	1	0				
3 ns	0	0	1	1				
4 ns	0	1	0	0				
5 ns	0	1	0	1				
6 ns	0	1	1	0				
7 ns	0	1	1	1				
Less than zero, > (–1 ns)	1	0	0	0				
–1 ns	1	0	0	1				
–2 ns	1	0	1	0				
–3 ns	1	0	1	1				
–4 ns	1	1	0	0				
–5 ns	1	1	0	1				
–6 ns	1	1	1	0				
–7 ns	1	1	1	1				
Input Hold times after Clock: Subfield B: Tenths of ns (bits 0 through 3)								
+/–0 ns	SEE Subfield table A				0	0	0	0
+/–0.1 ns					0	0	0	1
+/–0.2 ns					0	0	1	0
+/–0.3 ns					0	0	1	1
+/–0.4 ns					0	1	0	0
+/–0.5 ns					0	1	0	1
+/–0.6 ns					0	1	1	0
+/–0.7 ns					0	1	1	1
+/–0.8 ns					1	0	0	0
+/–0.9 ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	.
RFU	1	1	1	1	1	1	1	1

4.33 Bytes 36, PrefetchRead Latency. This byte describes the the latency from PrefetchRead Command to Data output of each physical bank on the VCSDRAM DIMM. If there is one physical bank on the module OR if there are two physical banks which have the same PrefetchRead Latency, then bits 0–3 are used to represent the latency for each physical bank. If the module has two physical banks of different latency, then bits 0–3 represent the latency for physical bank 1 and bits 4–7 represent the latency for physical bank 2.

For example:

# Banks	Latency of Bank 1	Latency of bank 2	Byte 36 contents
1	5 Clocks	N/A	0000 0101
2	5 Clocks	5 Clocks	0000 0101
2	5 Clocks	4 Clocks	0100 0101

PrefetchRead Latency (Clocks)		Table Subfield A: Prefetch Read Latency on Bank 1 –OR– Prefetch Read Latency on Bank 1 and 2 if both banks same depth, bits 0–3			
		Bit 3	Bit 2	Bit 1	Bit 0
Undefined	See Subfield B	0	0	0	0
1		0	0	0	1
2		0	0	1	0
:		:	:	:	:
7		0	1	1	1
8		1	0	0	0
9		1	0	0	1
10		1	0	1	0
11		1	0	1	1
12		1	1	0	0
13		1	1	0	1
14		1	1	1	0
15		1	1	1	1

PrefetchRead Latency (Clocks)	Table Subfield B: Prefetch Read Latency on Bank 2 (if different from Bank 1), bits 4–7				
	Bit 7	Bit 6	Bit5	Bit 4	
No 2nd Asymmetrical bank	0	0	0	0	See Subfield A
1	0	0	0	1	
2	0	0	1	0	
:	:	:	:	:	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

4.34 Bytes 37, tPCD. This byte identifies minimum required delay between Prefetch Command to Read/Write Command.

tPCD (Nanoseconds)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
31	0	0	0	1	1	1	1	1
32	0	0	1	0	0	0	0	0
33	0	0	1	0	0	0	0	1
34	0	0	1	0	0	0	1	0
35	0	0	1	0	0	0	1	1
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.35 Bytes 38, number of Segment addresses. This byte describes the number of segment addresses of each physical bank on the VCSDRAM DIMM. If there is one physical bank on the module OR if there are two physical banks which have the same number of Segment Addresses, then bits 0–3 are used to represent the number of Segment Addresses for each physical bank. If the module has two physical banks which have the different number of Segment Addresses, then bits 0–3 represent the number of Segment Addresses for physical bank 1 and bits 4–7 represent the number of Segment Addresses for physical bank 2.

For example;

# Banks	Number of Segment Addresses in Bank 1	Number of Segment Addresses in Bank 2	Byte 38 contents
1	2	N/A	0000 0010
2	2	2	0000 0010
2	2	4	0100 0010

# of Segment Addresses					Table Subfield A: No. of Segment addresses on Bank 1 –OR– PrefetchRead Latency on Bank 1 and 2 if both banks same depth, bits 0–3			
					Bit 3	Bit 2	Bit 1	Bit 0
Undefined					0	0	0	0
1					0	0	0	1
2					0	0	1	0
:					:	:	:	:
7	See Subfield B				0	1	1	1
8					1	0	0	0
9					1	0	0	1
10					1	0	1	0
11					1	0	1	1
12					1	1	0	0
13					1	1	0	1
14					1	1	1	0
15					1	1	1	1
# of Segment Addresses	Table Subfield B: Number of Segment Addresess on Bank 2 (if different from bank 1), bits 4–7							
	Bit 7	Bit 6	Bit5	Bit 4				
No 2nd Asymmetrical bank	0	0	0	0				
1	0	0	0	1				
2	0	0	1	0				
:	:	:	:	:				
7	0	1	1	1	See Subfield A			
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				
11	1	0	1	1				
12	1	1	0	0				
13	1	1	0	1				
14	1	1	1	0				
15	1	1	1	1				

4.36 Bytes 39, number of Channels This byte describes the numbr of Channels of each physical bank on the VCSDRAM DIMM. If there is one physical bank on the module OR if there are two physical banks which have the same number of Channels, then bits 0–3 are used to represent the number of channels for each physical bank. If the module has two physical banks of different number of Channels, then bits 0–3 represent the number of Channels for physical bank 1 and bits 4–7 represent the number of Channels for physical bank 2.

For example;

# Banks	# Channels in Bank 1	# Channels in Bank 2	Byte 39 contents
1	16	N/A	0000 0100
2	16	16	0000 0100
2	16	32	0101 0100

<table>
<tr><td rowspan="2"># of Channels</td><td colspan="4" rowspan="2"></td><td colspan="4">Table Subfield A: Number of Channels on Bank 1 –OR– Number of Channels on Bank 1 and 2 if both banks same depth, bits 0–3</td></tr>
<tr><td>Bit 3</td><td>Bit 2</td><td>Bit 1</td><td>Bit 0</td></tr>
<tr><td>Undefined</td><td colspan="4" rowspan="13">See Subfield B</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>4</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>128</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>256</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>512</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1024</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>2048</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4096</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>8192</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>16384</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>32768</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td rowspan="2"># of Channels</td><td colspan="4">Table Subfield B: Number of Channels on Bank 2 (if different from bank 1), bits 4–7</td><td colspan="4" rowspan="15">See Subfield A</td></tr>
<tr><td>Bit 7</td><td>Bit 6</td><td>Bit5</td><td>Bit 4</td></tr>
<tr><td>No 2nd Asymmetrical bank</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>4</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr>
<tr><td>128</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>256</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>512</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1024</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>2048</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4096</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>8192</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>16384</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>32768</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>

4.37 Bytes 40, Depth of Channels (bits) This field describes the depth of the channels on the module. If there is one physical bank on the module OR if there are two physical banks of the same depth of channels, then bits 0–3 are used to represent the depth of channels for each physical bank. If the module has two physical banks of different depth ofchannels, then bits 0–3 represent the depth of channels for physical bank 1 and bits 4–7 represent the depth of channels for physical bank 2.

For example;

# Banks	Depth of Channels in Bank 1	Depth of Channels in Bank 2	Byte 40 contents
1	128	N/A	0000 0111
2	128	128	0000 0111
2	128	64	0110 0111

# of Channels		Table Subfield A: Depth of Channels on Bank 1 –OR– Number of Channels on Bank 1 and 2 if both banks same depth, bits 0–3			
		Bit 3	Bit 2	Bit 1	Bit 0
Undefined	See Subfield B	0	0	0	0
2		0	0	0	1
4		0	0	1	0
:		:	:	:	:
128		0	1	1	1
256		1	0	0	0
512		1	0	0	1
1024		1	0	1	0
2048		1	0	1	1
4096		1	1	0	0
8192		1	1	0	1
16384		1	1	1	0
32768		1	1	1	1

# of Channels	Table Subfield B: Depth of Channels on Bank 2 (if different from bank 1), bits 4–7				
	Bit 7	Bit 6	Bit5	Bit 4	
No 2nd Asymmetrical bank	0	0	0	0	See Subfield A
2	0	0	0	1	
4	0	0	1	0	
:	:	:	:	:	
128	0	1	1	1	
256	1	0	0	0	
512	1	0	0	1	
1024	1	0	1	0	
2048	1	0	1	1	
4096	1	1	0	0	
8192	1	1	0	1	
16384	1	1	1	0	
32768	1	1	1	1	

4.38 + Bytes 41–61, Superset information. See appropriate Superset appendices.

4.39 Byte 62, Serial Presence Detect Revision: As SPD definition may be updated, it becomes necessary to identify the version of SPD which is being depicted. For keeping the consistency to SDRAM DIMM, use REV 2 for the initial release because the contents of the initial release of VCSDRAM SPD are based on REV 2 of SDRAM DIMM:

SPD Revision	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
Undefined	0	0	0	0	0	0	0	1
REV 2 (Initial Release)	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.