4.1.2.3 – Appendix C: Specific PD's for Fast Page Mode or Extended Data Out DRAM.

1 Introduction: This appendix describes the Presence Detects for Fast Page Mode DRAM and Extended Data Out (EDO) DRAM Modules. These PD's are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced; that is after the identification of the Fundamental Memory Type and before identification of whether there is any Superset Features presented. For convenience sake however, the complete address map is presented herein.

1.1 Address map: The following is the SPD address map for FPM and EDO. It describes where the individual LUT–Entries/bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfgr	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	3
4	# Column Addresses on this assembly	
5	# DRAM Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	RAS# access time of this assembly	4
10	CAS# access time of this assembly	4
11	DIMM Configuration type (Non–parity, Parity, ECC)	
12	Refresh Rate/Type	4,5
13	DRAM width, Primary DRAM	
14	Error Checking DRAM data width	
15–31	Reserved for future offerings	
32	Superset Memory Type (may be used in future)	
33–62	Superset Memory Specific Features (may be used in future)	
63	Checksum for bytes 0–62	
64–71	Manufacturers JEDEC ID code per JEP–106	6
72	Manufacturing location	6
73–90	Manufacturer's Part Number	6
91–92	Revision Code	6
93–94	Manufacturing date	6
95–98	Assembly Serial Number	6
99–125	Manufacturer Specific Data	6
126–127	Reserved	
128–255	Open User Free–Form area$not defined	

notes:

1) This will be 128 bytes for FPM and EDO DRAM

2) This will be 256 bytes, represented as 08h. See below.

3) High order bit defines is assembly has "redundant" addressing (if set to "1", highest order RAS# address must be re–sent as highest order CAS# address.)

4) From data sheet.

5) High order bit (MSB) is Self Refresh $flag'. If bit seven is "1", assembly supports self refresh.

6) Per the JEDEC spec, these are optional.

Downloaded by F L (mgrglfau@sharklasers.com) on Aug 5, 2025, 4:20 pm PDT

2 **Bytes 0–2,** For Reference: Descriptions of bytes 0–1 can be found in the main body of the SPD standard, and byte 2 is detailed in **appendix A** to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 **BYTE 0**, From General SPD Standard, Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 **Byte 1**, From General SPD Standard, Total SPD Memory Size: This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

Downloaded by F L (mgrglfau@sharklasers.com) on Aug 5, 2025, 4:20 pm PDT

2.3 Byte 2, From Appendix A, Memory Type: This byte describes the fundamental memory type (or technology) implemented on the module:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
Standard FPM DRAM	0	0	0	0	0	0	0	1
EDO	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

3 Data Type(s): Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.

4 The following PD bytes are those specific to modules implementing Fast Page Mode and EDO DRAM technology. Note that full descriptions start at byte 3 and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology.

4.1 Byte #3, Number of ROW Addresses: This first field describes the number of Row Addresses in the DRAM array:

No. of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
Undefined	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
12(redundant)	1	0	0	0	1	1	0	0
13(redundant)	1	0	0	0	1	1	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
126(redundant)	1	1	1	1	1	1	1	0
127(redundant)	1	1	1	1	1	1	1	1

Bit7: "0" indicates normal addressing; "1" indicates redundant addressing

Downloaded by F L (mgrglfau@sharklasers.com) on Aug 5, 2025, 4:20 pm PDT

4.2 Byte #4, Number of COLUMNs Addresses: This field describes the number of COLUMN addresses in the module's DRAM array:

Number of COLUMN Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.3 Byte #5, Number of Banks: This field describes the number of banks on the DRAM Module:

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

Downloaded by F L (mgrglfau@sharklasers.com) on Aug 5, 2025, 4:20 pm PDT

4.4 **Bytes 6 & 7,** Module Data Width: Bytes 6 and 7 are used to designate the modules data width. The data width is presented as a 16 bit word; bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits wide, byte 7 will be 00h. If the data width is 256 bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width. For example, if the module's data width is:

then byte 7 is	and byte 6 is:
0000 0000	0100 0000
0000 0000	0100 1000
0000 0010	0100 0000

Byte 6:

Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

4.4.1 Byte 7, Module Data Width Continued: This byte will be left at 00h if the original module data width is less than 256 bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6.

Module Data Width Cont.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.

4.5 Byte 8, Module Interface Levels: This field describes the module's voltage interface:

Voltage Interface	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
New Table	1	1	1	1	1	1	1	1

Downloaded by F L (mgrglfau@sharklasers.com) on Aug 5, 2025, 4:20 pm PDT

4.6 Byte 9, RAS Access Time (tRAC): This field describes the module's RAS access time:

RAS Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1ns	0	0	0	0	0	0	0	1
2ns	0	0	0	0	0	0	1	0
3ns	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
50ns	0	0	1	1	0	0	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
60ns	0	0	1	1	1	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
70ns	0	1	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
80ns	0	1	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
254ns	1	1	1	1	1	1	1	0
255ns	1	1	1	1	1	1	1	1

4.7 Byte 10, CAS Access Time (tCAC): This field describes the module's CAS access time:

CAS Access Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1ns	0	0	0	0	0	0	0	1
2ns	0	0	0	0	0	0	1	0
3ns	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
10ns	0	0	0	0	1	0	1	0
11ns	0	0	0	0	1	0	1	1
12ns	0	0	0	0	1	1	0	0
13ns	0	0	0	0	1	1	0	1
14ns	0	0	0	0	1	1	1	0
15ns	0	0	0	0	1	1	1	1
16ns	0	0	0	1	0	0	0	0
17ns	0	0	0	1	0	0	0	1
18ns	0	0	0	1	0	0	1	0
19ns	0	0	0	1	0	0	1	1
20ns	0	0	0	1	0	1	0	0
21ns	0	0	0	1	0	1	0	1
22ns	0	0	0	1	0	1	1	0
23ns	0	0	0	1	0	1	1	1
24ns	0	0	0	1	1	0	0	0
25ns	0	0	0	1	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254ns	1	1	1	1	1	1	1	0
255ns	1	1	1	1	1	1	1	1

Downloaded by F L (mgrglfau@sharklasers.com) on Aug 5, 2025, 4:20 pm PDT

4.8 Byte 11, Module Configuration type: This field describes the module's error detection and or correction schemes:

Error Det/Cor	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	1

4.9 Byte 12, Refresh Rate/Type: This field describes the module's refresh rate and type:

Refresh Period	Bit 7, Self Refresh Flag	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal (15.625 us)	0	0	0	0	0	0	0	0
Reduced (.25x)...3.9us	0	0	0	0	0	0	0	1
Reduced (.5x)...7.8us	0	0	0	0	0	0	1	0
Extended (2x)...31.3us	0	0	0	0	0	0	1	1
Extended (4x)...62.5us	0	0	0	0	0	1	0	0
Extended (8x)...125us	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
TBD	0	0	0	0	0	1	1	1
TBD	0	0	0	0	1	0	0	0
TBD	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
Self Refresh Entries								
Normal (15.625us)	1	0	0	0	0	0	0	0
Reduced (0.25x)...3.9us	1	0	0	0	0	0	0	1
Reduced (0.5x)...7.8us	1	0	0	0	0	0	1	0
Extended (2x)...31.3us	1	0	0	0	0	0	1	1
Extended (4x)...62.5us	1	0	0	0	0	1	0	0
Extended (8x)...125us	1	0	0	0	0	1	0	1
TBD	1	0	0	0	0	1	1	0
TBD	.	.	.	.	.	.	.	.
TBD	.	.	.	.	.	.	.	.
TBD	1	1	1	1	1	1	1	0
TBD	1	1	1	1	1	1	1	1

Downloaded by F L (mgrglfau@sharklasers.com) on Aug 5, 2025, 4:20 pm PDT

4.10 Byte 13, DRAM width, Primary DRAM: This field describes the width of the primary DRAMs used on the module. The primary DRAM is that which is used for data; examples of primary (data) DRAM widths are x4, x8, x16, x32. Note that if the module is made with DRAMs which provide extra bits for data and error checking e.g. x9, x18, x36, then it is also designated in this field. Examples using x72 modules include:

Module width	Primary Data DRAM Width	Error Checking DRAM Width	Qty Primary Data DRAMs	Byte 13 (Binary)
x72	x9	—	8	0000 1001
x72	x8	x8	9	0000 1000
x72	x16	x1	4	0001 0000

DRAM Width, Primary DRAM	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
15	0	0	0	0	1	1	1	1
16	0	0	0	1	0	0	0	0
17	0	0	0	1	0	0	0	1
18	0	0	0	1	0	0	1	0
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

4.11 Byte 14, Error Checking DRAM data width: If the module incorporates error checking and if the primary data DRAM does not include these bits; i.e. there are separate error checking DRAMs, then the error checking DRAM's width is expressed in this byte. Examples of error checking DRAM widths include x1, x4, x8. For Example:

Module width	Primary DRAM Width	Error Checking DRAM Width	Qty of Error Checking DRAMs	Byte 14 (Binary)
x72	x9	—	—	0000 0000
x72	x8	x8	1	0000 1000
x72	x16	x1	8	0000 0001

DRAM Width Error Checking DRAM	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
255	1	1	1	1	1	1	1	1

Downloaded by F L (mgrglfau@sharklasers.com) on Aug 5, 2025, 4:20 pm PDT

4.12 Bytes 15–31: Open. There are no defined PD settings for these bytes.

4.13 Bytes 32 through 62, Superset information: If a superset technology is developed and is completely backward compatible, it may be specified and its SPD may be defined in bytes 32 through 62.

4.14 Byte 63, Checksum for bytes 0–62: The Checksum will be calculated using the procedure defined in the SPD General Standard, Sec. 4.1.2, Pars. 4.3 & 5.7.

5 From the general SPD standard: The descriptions of bytes 64–127 are repeated here For Reference ONLY. Manufacturers MAY include information which is pertinent to their particular modules, place and date of manufacture, etc. If a module manufacturer decides to write data into bytes 64–127, they must follow the format and order presented below. If a module manufacturer chooses not to include the data outlined below, they must leave bytes 64–127 unprogrammed; blank state of these bytes may be 00h or FFh. Detailed implementation of bytes 64–127 is detailed below in paragraphs 5.X:

5.1 Bytes 64–71: Manufacturers ID code per EIA/JEP106. Manufacturers of a given module may include their identifier per Jedec spec JEP106. 00h is not allowed and FFh indicated continuation. The first byte is utilized, the second byte filling. Unused locations/bytes should be FFh.

5.2 Byte 72: Manufacturing Location. Manufacturers may include an identifier which uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

5.3 Bytes 73–90: Manufacturer's Part Number: Manufacturers may include their part number in 6–bit ASCII format within these bytes.

5.4: Bytes 91–92: Revision Code: This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

5.5 Bytes 93–94: Date of Module Manufacture: The module manufacturer may include a date code for the module. Specifically, byte 93 may contain the year in Binary and byte 94 may contain the week in Binary.

5.6 Bytes 95–98: Module Serial Number: The supplier may include a serial number for module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

5.7 Bytes 99–125: Manufacturers specific data, open area. The module manufacturer may add any additional information desired into the module within these locations.

5.8 Bytes 126–127: Reserved. These bytes are reserved and cannot be later allocated.

Downloaded by F L (mgrglfau@sharklasers.com) on Aug 5, 2025, 4:20 pm PDT