4.1.1 Memory Module Nomenclature

4.1.1.1 - Purpose

The purpose of this standard is to establish a format for a number system which defines the format of a number which is an architectural description of multi- chip memory modules. It is intended to be used with but not restricted to modules made with DRAM devices.

4.1.1.2 - Number Format

The description number designation shall consist of 8 fields with the form nnSccbbDttIpp where :
nn = the number of longitudinal positions on the module: 4, 5, 8, 9.
S = the number of sides on the module stated as "single or double" : S, D
cc = the capacity of the memory chip stated in terms of the log(2) of the capacity (i.e.- the number of address bits needed for the chip): 16, 18, 20, 22
bb = the number of data bits in the interface: 1, 2, 4, 5, 8, 9, 10, 17
D = the data interface configuration, common, separate, or mixed: C, S, M
tt = total number of words stated as log(2) of the capacity: 16- - 26
I = mechanical interface: P = pins, E = edge card connector
pp = number of pins or pads

4.1.1.3 - Number Example

A module with the following attributes:
9 chips long
Double sided
18 bit data interface
Separate I/O for parity bits, common I/O for other bits
1M X 1 memory chips
Pin interface
Architectural number: 9D2018M20P40